

# CHIP LEGISLATIVE ENDEAVORS IN THE UNITED STATES AND EUROPEAN UNION: A COMPARATIVE ANALYSIS BASED ON CHINA'S DISRUPTIVE PRODUCTION TECHNOLOGIES

Alvin Hoi-Chun Hung<sup>†</sup>

## Abstract

*Based on a comparison between the CHIPS and Science Act of 2022 (the CHIPS Act) in the United States and the European Chips Act of 2023 (the EU Chips Act), this article explores the latent inefficacy of both acts, given the potential of the development of China's disruptive technology to revolutionize chip manufacturing. The study contends that traditional approaches outlined in both acts might be rendered outdated by emerging technology-based paradigms, particularly those embodied by existing multiple patterning and emerging particle accelerator technologies. By elucidating the transformative potential inherent in multiple patterning and particle acceleration together with the pioneering Steady-State Microbunching (SSMB) technologies, this analysis offers a discerning evaluation of the effectiveness of these chip laws in navigating the intricate dynamics of contemporary semiconductor fabrication. Two analytical frameworks, the disruptive innovation and path dependency theories, can offer valuable insight in examining the ramifications of the CHIPS Act. In conclusion, this article presents a fine-tuned viewpoint on the intersection of legislative endeavors and technological advancements in the semiconductor industry, thereby contributing to a deeper comprehension of the intricate interplay between policy frameworks and disruptive innovation.*

## Keywords

The CHIPS and Science Act, The European Chips Act, Multiple patterning, Particle Accelerators

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<sup>†</sup> Dr. Alvin Hoi-Chun Hung is an active sociolegal researcher who has published several papers in journals such as *University of Illinois Journal of Law, Technology and Policy*, *Qualitative Research Journal*, *Law and Humanities*, *Asian Journal of Law and Policy*, and *Asian Journal of Law and Society*. He is currently a postdoctoral fellow at the College of Law, Australian National University. He has a DPhil from the University of Oxford and an LLM (Master of Law) from the London School of Economics and Political Science.

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## I. INTRODUCTION

Huawei’s Mate 60 Pro, released in August 2023, utilizes 7nm chips manufactured within China despite restrictions from the U.S. on the import of the most advanced chipmaking equipment to China.<sup>1</sup> This accomplishment is attained by utilizing a method known as multiple patterning that relies on Deep Ultraviolet (DUV) lithography with lower resolution compared to the more advanced Extreme Ultraviolet (EUV) technology.<sup>2</sup> While DUV lithography is typically used for larger chips, multiple patterning breaks down the circuit patterns into smaller sections, each exposed to DUV light multiple times to produce much smaller chips.<sup>3</sup> Although this approach comes with the drawbacks

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1. Douglas B. Fuller, *Tech War or Phony War? America’s Porous Controls on Semiconductor Fabrication Equipment and China’s Response*, 78 CHINA LEADERSHIP MONITOR, 9–10 (Dec. 1, 2023) (stating that the U.S. limited to sales to China and that the Mate 60 Pro uses a 7-nm chipset produced in Shanghai).

2. Xiaolin Wang, et al., *Trends in Photoresist Materials for Extreme Ultraviolet Lithography: A Review*, 67 MATERIALS TODAY 299, 299, 318 (July–Aug. 2023).

3. See generally Guojin Chen, et al. *GPU accelerated matrix cover algorithm for multiple patterning layout decomposition*, ARXIV (Mar. 25, 2023), <https://arxiv.org/abs/2303.14335> [<https://perma.cc/RU49-A9W2>] (discussing multiple patterning lithography); *Enabling Advanced ICs with Multiple Patterning*, LAM RESEARCH (June 12, 2017), <https://newsroom.lamresearch.com/Enabling-Advanced-ICs-with-Multiple-Patterning?blog=true> [<https://perma.cc/QGP6-ESKY>].

of higher production costs and lower success rates, China manages to sustain progress in chip manufacturing despite the continuation of American sanctions.<sup>4</sup>

In an era characterized by the relentless pursuit of scientific progression, the microprocessor industry, commonly referred to as the “chip industry,” emerges as a pivotal catalyst of technological advancement.<sup>5</sup> Serving as the fundamental nucleus of contemporary electronic systems, these chips constitute the bedrock of an impressive spectrum of devices, ranging from ubiquitous handheld devices such as smartphones to sophisticated machinery employed in space exploration.<sup>6</sup>

For the sake of clarity, a preliminary differentiation of terms is necessary. The nomenclature encompassing “chip,” “semiconductor,” and “microprocessor” within the domain of the chip industry serves to demarcate discrete attributes and functionalities.<sup>7</sup> The term “chip” commonly designates a diminutive, planar piece of semiconductor material, predominantly silicon, serving as the substrate for the fabrication of integrated circuits, including microprocessors and memory chips.<sup>8</sup> In contradistinction, “semiconductor” not only characterizes the material itself, exemplified by silicon, possessing electrical conductivity intermediaries between conductors and insulators,<sup>9</sup> but extends its purview to encompass devices originating from this material, constituting a diverse array of chips integral to electronic systems.<sup>10</sup> Conversely, a “microprocessor” signifies a specific subclass of chips endowed with the function of a central processing unit (CPU) in electronic apparatus, undertaking the execution of instructions and the orchestration of varied operations within the system.<sup>11</sup> Consequently, this article will follow the common nomenclature which delineates “chip” as a broad categorization, “semiconductor” as an overarching term encompassing both material and derived devices, and “microprocessor” as a specialized classification specifying a chip type pivotal to computing architectures.<sup>12</sup>

While most chips were invented and developed in the U.S., the manufacturing of high-end chips is currently dominated by two companies: ASML (Advanced Semiconductor Materials Lithography), which produces the

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4. Jimmy Goodrich, *China's Evolving Semiconductor Strategy*, UNIV. OF CAL. INST. ON GLOB. CONFLICT AND COOP. (May 29, 2024) <https://ucigcc.org/blog/chinas-evolving-semiconductor-strategy/> [<https://perma.cc/VVT8-G64Y>]

5. CHRIS MILLER, *CHIP WAR: THE FIGHT FOR THE WORLD'S MOST CRITICAL TECHNOLOGY* (2022).

6. *The Basics of Microchips*, ASML, <https://www.asml.com/en/technology/all-about-microchips/microchip-basics> [<https://perma.cc/P4KT-GDYW>] (last visited Sept. 12, 2024).

7. *See Comparison Between Chips, Semiconductors and Integrated Circuits*, IBE ELC. (Sept. 18, 2023), [www.pcbaaa.com/comparison-between-chips-semiconductors-and-integrated-circuits/](http://www.pcbaaa.com/comparison-between-chips-semiconductors-and-integrated-circuits/) [<https://perma.cc/QGL9-Z9TF>] (explaining that a “chip” is a “silicon chip containing an integrated circuit,” a “semiconductor” is a “material whose electrical conductivity . . . is between that of a conductor and an insulator,” and a “microprocessor” is a specific type of integrated circuit that serves as the central processing unit (CPU) of a computer or other digital devices).

8. ASML, *supra* note 6.

9. IBE ELC., *supra* note 7.

10. CHRISTOPHER SIU, *ELECTRONIC DEVICES, CIRCUITS, AND APPLICATIONS* 35 (Springer Int'l Publishing 2022).

11. MICHAEL S. MALONE, *THE MICROPROCESSOR: A BIOGRAPHY*, 5–34 (1995).

12. ASML, *supra* note 6; Josh Schneider & Ian Smalley, *What is a Microprocessor?*, IBM (June 10, 2024), <https://www.ibm.com/think/topics/microprocessor> [<https://perma.cc/E6RG-3XB2>].

most advanced tools and equipment, and TSMC (Taiwan Semiconductor Manufacturing Company Limited), which can mass-produce chips.<sup>13</sup> Both of these market leaders are non-American companies.<sup>14</sup> This raises an important question: Can U.S. laws or executive measures bring the high-end chip manufacturing process back to American soil?

Recognizing the critical role of chips in sustaining economic growth and national security, the U.S. Congress passed the CHIPS and Science Act of 2022 (the CHIPS Act) to bolster domestic semiconductor manufacturing and technological innovation.<sup>15</sup> The Act provides a specific amount of \$52.7 billion, out of a total provision of \$280 billion, in funding for chip research, development, manufacturing, and workforce development.<sup>16</sup> The Act is a bipartisan bill supported by both Democrats and Republicans, and it is seen as a major victory for the Biden administration's effort to prioritize the U.S. semiconductor industry.<sup>17</sup>

The CHIPS Act is supposedly a landmark piece of legislation representing a significant investment by the U.S. government in the chip industry.<sup>18</sup> The Act has the potential to address a number of challenges, including the global semiconductor supply chain crisis and the decline of U.S. semiconductor manufacturing competitiveness.<sup>19</sup> The CHIPS Act also has the potential to revolutionize chip manufacturing by adopting particle accelerator technology.<sup>20</sup> However, there are some challenges associated with the CHIPS Act. One major challenge is that it will take time for the Act to have a significant impact on chip manufacturing in the U.S.<sup>21</sup> Another major challenge is that the Act's

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13. See David Sacks & Seaton Huang, *Onshoring Semiconductor Production: National Security Versus Economic Efficiency*, COUNCIL ON FOREIGN RELATIONS (Apr. 17, 2024, 1:52 PM), <https://www.cfr.org/article/onshoring-semiconductor-production-national-security-versus-economic-efficiency> [https://perma.cc/6829-NF8F] (stating that while semiconductors were invented in the U.S. and U.S. companies design the most advanced chips, they outsource actual production, and TSMC dominates semiconductor manufacturing); Fuller, *supra* note 1, at 3 (explaining that ASML dominates the market for lithography equipment).

14. Fuller, *supra* note 1, at 3; David Sacks & Seaton Huang, *supra* note 13.

15. *FACT SHEET: CHIPS and Science Act Will Lower Costs, Create Jobs, Strengthen Supply Chains, and Counter China*, THE WHITE HOUSE (Aug. 9, 2022), <https://www.whitehouse.gov/briefing-room/statements-releases/2022/08/09/fact-sheet-chips-and-science-act-will-lower-costs-create-jobs-strengthen-supply-chains-and-counter-china/> [https://perma.cc/4S6L-EVAT]; CHIPS and Science Act, Pub. L. No. 117-167, § 10109, 136 Stat. 1366.

16. Michael A. Peters, *Semiconductors, Geopolitics and Technological Rivalry: The US CHIPS & Science Act, 2022*, 55 EDUC. PHIL. AND THEORY 1642, 1644 (2023); Makena Kelly, *Biden signs \$280 billion CHIPS and Science Act*, THE VERGE (Aug. 9, 2022, 9:57 AM), <https://www.theverge.com/2022/8/9/23298147/biden-chips-act-semiconductors-subsidies-ohio-arizona-plant-china> [https://perma.cc/M56A-5EX3].

17. Peters, *supra* note 16, at 1644.

18. See THE WHITE HOUSE, *supra* note 15 (touting billions of dollars in investment in the semiconductor industry by the U.S. government).

19. Gary Clyde Hufbauer & Megan Hogan, *CHIPS Act Will Spur US Production but Not Foreclose China*, PETERSON INST. FOR INT'L ECON. (Oct. 2022), <https://www.piie.com/sites/default/files/2022-10/pb22-13.pdf> [https://perma.cc/H2ZB-CBXE].

20. Michael Taylor, *The US CHIPS and Science Act of 2022*, 48 PUB. AFF. F. 874, 876 (Sept. 2023).

21. Binglei Zhou, *The Impact of the U.S. Chip4 Alliance, and China How to Respond It*, 1 TRANSACTIONS ON SOC. SCI., EDUC. AND HUMAN. RSCH. 407, 409 (2023).

geographical manufacturing restrictions could limit its effectiveness in addressing the global semiconductor supply chain crisis.<sup>22</sup>

One year after the enactment of the CHIPS Act in the U.S., the European Chips Act (EU Chips Act) emerged from the European Chips Act Initiative (ECAI) on the other side of the Atlantic Ocean.<sup>23</sup> ECAI is a European Commission initiative aimed at fostering investment in semiconductor manufacturing and research within the European Union (EU).<sup>24</sup> The initiative was announced in September 2021 and enacted as the EU Chips Act in September 2023.<sup>25</sup> The EU Chips Act will be implemented through a combination of EU funding, national funding, and private investment.<sup>26</sup> The European version of the promotion of local chip manufacturing has specific provisions to plan to increase the EU's chip production capacity to 20% of the global market by 2030.<sup>27</sup>

Both the CHIPS Act and the EU Chips Act are formulated based on the status quo of the prevailing chip manufacturing technology.<sup>28</sup> However, the emerging disruptive scientific development in chip manufacturing based on multiple patterning and the long-existing particle accelerator technology can be used to produce chips more efficiently.<sup>29</sup>

Multiple patterning in chip manufacturing is an existing but improved technique that involves splitting a single layer of a semiconductor design into multiple exposures, allowing for the creation of smaller features than traditional lithography methods can achieve alone.<sup>30</sup> Another emerging technique, particle accelerators, have already been used in a variety of industries, including medicine, research, and manufacturing.<sup>31</sup> Traditional semiconductor fabrication methods are complex and expensive, requiring much energy and water.<sup>32</sup> While

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22. See *id.* at 408 (stating that the CHIPS Act “require[s] U.S. semiconductor factories to obtain a license to export materials for the manufacturing equipment of related semiconductors to China” and “restrict[s] Americans from engaging in chip manufacturing-related work in China”).

23. See Bernhard Dachs, *The European Chips Act*, FIW: POL’Y BRIEF NO. 58 (Feb. 2023) (explaining that the European Chips Act was introduced in 2021 and can “be seen as a reaction to similar initiatives in other countries”).

24. *Id.* at 1.

25. *Ibid.*; *European Chips Act*, EUR. COMM’N, [https://commission.europa.eu/strategy-and-policy/priorities-2019-2024/europe-fit-digital-age/european-chips-act\\_en](https://commission.europa.eu/strategy-and-policy/priorities-2019-2024/europe-fit-digital-age/european-chips-act_en) [<https://perma.cc/46YW-ND73>] (last visited Sept. 15, 2024).

26. EUROPEAN COMM’N, *supra* note 25.

27. Bob Hancké & Angela Garcia Calvo, *Mister Chips Goes to Brussels: On the Pros and Cons of a Semiconductor Policy in the EU*, 13 GLOBAL POLICY 585, 590 (2022).

28. See Sujai Shivakumar et al., *A World of Chips Acts: The Future of U.S.-EU Semiconductor Collaboration*, CTR. FOR STRATEGIC & INT’L STUD. (Aug. 20, 2024), <https://www.csis.org/analysis/world-chips-acts-future-us-eu-semiconductor-collaboration> [<https://perma.cc/76EC-8JUZ>] (explaining that both aim to spur domestic chip manufacturing by allocating most of the allocated money to those facilities, and most of the remainder is given to research and development).

29. R. J. England et al., *Progress in Developing an Accelerator on a Chip*, 13 INT’L PARTICLE ACCELERATOR CONF. 16, 16 (2022); David Z. Pan et al., *Pushing Multiple Patterning in Sub-10nm: Are We Ready?* IEEE XPLORÉ (2015), <https://ieeexplore.ieee.org/document/7167382> [<https://perma.cc/2HLR-DRZV>].

30. David Z. Pan et al., *supra* note 29.

31. *Particle Accelerators and Radiation Research*, EPA, <https://www.epa.gov/radtown/particle-accelerators-and-radiation-research> [<https://perma.cc/6LYA-R7VD>] (last updated Aug. 21, 2024).

32. Marcello Ruberti, *The Chip Manufacturing Industry: Environmental Impacts and Eco-Efficiency Analysis*, 858 SCI. OF THE TOTAL ENV’T 1, 2 (2023).

still in the early stage of development, particle accelerator technology can be utilized to create semiconductors more efficiently and effectively, and it could also reduce the environmental impact of chip manufacturing.<sup>33</sup> This revolutionary technology can significantly impact the efficacy of the CHIPS Act and the EU Chips Act.<sup>34</sup>

This article analyzes the CHIPS Act and the EU Chips Act in the context of existing multiple patterning techniques and emerging particle accelerator technology. It is organized into distinct parts and sections for clarity and depth of coverage. Part I introduces the acts, setting the stage for subsequent discussions. Part II offers an expansive overview of the CHIPS Act, encompassing legislative objectives, provisions, historical context, and the allocation of federal subsidies to bolster chip manufacturing in the U.S. In Part III, the EU Chips Act's provisions are scrutinized alongside prevailing industry trends, evaluating its potential to mitigate current supply chain disruptions. Part IV examines the process of chip manufacturing with reference to major players such as ASML and TSMC. It reviews the principles of particle accelerator technology, delineating its advantages over conventional semiconductor fabrication methods and exploring its transformative potential in revolutionizing chip production efficiency and capabilities. Part V critically assesses the technological readiness and infrastructure prerequisites for the adoption of particle accelerator technology in chip manufacturing. In Part VI, a comprehensive analysis is provided, addressing funding limitations, semiconductor manufacturing locations, and the resulting implications for global semiconductor supply chain dynamics within the geographical restrictions outlined in the Act. The penultimate section undertakes a comparative examination of the CHIPS Act in the U.S. and the EU Chips Act in Europe, proposing potential reforms for the former. Finally, the article provides recommendations to improve the CHIPS Act with a view to the competitiveness of the U.S. in chip manufacturing.

## II. OVERVIEW OF THE CHIPS AND SCIENCE ACT OF 2022

The CHIPS and Science Act (the CHIPS Act) is a U.S. federal statute enacted by the 117th U.S. Congress and signed into law by President Biden on August 9, 2022.<sup>35</sup> The acronym “CHIPS,” as employed within the nomenclature of the CHIPS Act, should not be misconstrued as a reference to the common connotation of “chips,” which signifies the integrated circuits in electronic devices.<sup>36</sup> Rather, in this legislative context, “CHIPS” is an abbreviation denoting “Creating Helpful Incentives to Produce Semiconductors.”<sup>37</sup>

This bipartisan legislation comes in response to a significant disruption in the semiconductor supply chain and represents the political concerns on how

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33. England et al., *supra* note 29.

34. *See id.* (explaining that the technological advancements can lead to lower costs and higher power).

35. CHIPS and Science Act, Pub. L. No. 117-167, § 10109, 136 Stat. 1366.

36. *See id.* at § 102(a)(1) (establishing “Creating Helpful Incentives to Produce Semiconductors” as “CHIPS”).

37. *Ibid.*

best to fortify U.S. competitiveness in an industry deemed crucial for national and economic security.<sup>38</sup> The capacity for chip manufacturing in the U.S. has declined from nearly 40% of global supply in 1990 to its current standing at 12%.<sup>39</sup> There is a critical need to help the chip manufacturers in the U.S.<sup>40</sup>

The CHIPS Act marks a watershed moment in the history of American technological policy.<sup>41</sup> Enacted to bolster domestic semiconductor manufacturing and foster innovation, this legislation represents a concerted effort to secure the nation's competitive edge in an increasingly technology-dependent world.<sup>42</sup> With the global semiconductor industry experiencing unprecedented growth, the Act's provisions seek to address critical gaps in the supply chain and pave the way for sustained leadership in cutting-edge technologies.<sup>43</sup> This essay examines the CHIPS Act's key components, objectives, and potential impacts, shedding light on its significance for the future of American innovation and economic resilience.

#### A. *Legislative Objectives and Provisions*

The CHIPS Act constitutes an ambitious legislative initiative that transcends its statutory dimensions, embodying a substantial commitment to bolstering the American semiconductor sector.<sup>44</sup> This legislative endeavor encapsulates a strategic infusion of resources, encompassing financial, technological, and infrastructural components, aimed at fortifying the domestic semiconductor industry's competitive edge in the global supply chain of chips.<sup>45</sup> The Act stands as a testament to a proactive policy approach, reflecting a discerning recognition of the pivotal role that semiconductor technologies play in national security, economic resilience, and technological innovation.<sup>46</sup> It signifies an overarching vision to propel the U.S. into a position of leadership and self-sufficiency within the critical business of semiconductor manufacturing and research.<sup>47</sup>

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38. EMILY G. BLEVINS ET AL., CONG. RSCH. SERV., FREQUENTLY ASKED QUESTIONS: CHIPS ACT OF 2022 PROVISIONS AND IMPLEMENTATION 2–4 (2023); THE WHITE HOUSE, *supra* note 15.

39. PRESIDENT'S COUNCIL OF ADVISORS ON SCI. AND TECH., REP. TO THE PRESIDENT: REVITALIZING THE U.S. SEMICONDUCTOR ECOSYSTEM 2 (2022).

40. *See id.* at 11–12 (explaining that semiconductors are critical to national security and economic interests, the share of semiconductors manufactured in the U.S. has declined long-term, and the need for action is urgent).

41. *See* BLEVINS ET AL., *supra* note 38, at 1 (noting that the CHIPS Act appropriates \$52.7 billion towards the U.S. semiconductor industry).

42. Yadong Luo & Ari Van Assche, *The Rise of Techno-Geopolitical Uncertainty: Implications of the United States CHIPS and Science Act*, 54 J. INT'L BUS. STUD. 1423, 1425–26 (2023).

43. *Ibid.*

44. Justin Badlam et al., *The CHIPS and Science Act: Here's What's in It*, MCKINSEY (Oct. 4, 2022), <https://www.mckinsey.com/industries/public-sector/our-insights/the-chips-and-science-act-heres-whats-in-it#/> [<https://perma.cc/R88W-JE2W>].

45. *Id.*

46. *New Chips Act Could Become a \$280 Billion Boondoggle*, BLOOMBERG (Aug. 1, 2022), <https://www.bloomberg.com/opinion/articles/2022-08-01/chips-and-science-act-could-become-a-280-billion-boondoggle> [<https://perma.cc/VB7T-T7C7>].

47. *Id.*

The CHIPS Act allocates a substantial budgetary appropriation totaling about \$280 billion across the forthcoming five years.<sup>48</sup> Predominantly, an allocation of \$200 billion is designated for the facilitation of scientific research and development endeavors, as well as the advancement of commercialization initiatives.<sup>49</sup> A notable portion, amounting to \$52.7 billion, is earmarked for the augmentation of semiconductor manufacturing processes, alongside parallel investment in research and development activities, complemented by strategic initiatives aimed at workforce development.<sup>50</sup> Additionally, an appreciable provision of \$24 billion is stipulated in the form of tax credits specifically tailored to incentivize and fortify the production of semiconductor chips.<sup>51</sup> Furthermore, an allocation of \$3 billion is earmarked for programs expressly designed to propel pioneering technologies and fortify the robustness of wireless supply chains.<sup>52</sup>

The CHIPS Act embodies a strategic legislative initiative meticulously crafted to augment competitive acumen, innovative capacity, and national security posture in the U.S.<sup>53</sup> At its core lies a deliberate emphasis on catalyzing investments in fortifying the nation's domestic semiconductor manufacturing prowess.<sup>54</sup> This imperative extends to a concerted revitalization of research and development endeavors, culminating in the commercialization of cutting-edge technologies spanning diverse domains, including, but not limited to, quantum computing, artificial intelligence (AI), sustainable energy solutions, and nanotechnology.<sup>55</sup> This comprehensive undertaking also envisions the establishment of novel high-technology hubs across varied regions, concomitant with the cultivation of a more expansive and inclusive workforce specialized in science, technology, engineering, and mathematics (STEM) disciplines.<sup>56</sup> Through strategic investments in semiconductor manufacturing and the promotion of scientific inquiry, the Act endeavors to fortify the bedrock of American innovation.<sup>57</sup>

### B. *Historical Background and Impetus for Enactment*

Semiconductors or chips assume an indispensable role in an extensive array of products and systems.<sup>58</sup> This escalating significance makes the U.S. susceptible to supply chain disruptions and reliance on foreign chip

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48. *Id.*

49. Jianxi Luo, *Close the Gap in the US CHIPS and Science Law*, 610 NATURE 34, 34 (2022).

50. Hufbauer & Hogan, *supra* note 19, at 1.

51. *See* THE WHITE HOUSE, *supra* note 15 (mentioning a 25% tax credit for capital expenses).

52. *Id.*

53. *See id.* (discussing the strategic plan for the CHIPS and Science Act).

54. *Id.*

55. *See* Badlam et al., *supra* note 44 (discussing the various applications of the CHIPS and Science Act).

56. *See id.* (discussing the CHIPS and Science Act's goals for the future).

57. *Id.*

58. *See* Ana Swanson, *The CHIPS Act is About More than Chips: Here's What's in It*, THE ECONOMIC TIMES (Mar. 2, 2023), <https://economictimes.indiatimes.com/small-biz/trade/exports/insights/the-chips-act-is-about-more-than-chips-heres-whats-in-it/articleshow/98353142.cms?from=mdr> [https://perma.cc/EF3J-CLGF].

manufacturers.<sup>59</sup> China presently exerts a commanding influence over the global semiconductor supply chain, an ascendancy largely underpinned by substantial investments in manufacturing infrastructures typified by entities like the Semiconductor Manufacturing International Corporation (SMIC).<sup>60</sup> The nation's influence spans across the spectrum of fabrication, assembly, and testing.<sup>61</sup> Moreover, China stands as a prominent consumer and exporter of semiconductor chips, fortified by a resilient ecosystem of suppliers, a skilled labor force, and comprehensive government backing.<sup>62</sup>

Following the rise of China as a prominent manufacturing hub in recent years, the U.S. has experienced a discernible decline in its preeminent position on the global stage in chip manufacturing.<sup>63</sup> This decline can be attributed to a confluence of factors, including the lure of lower labor costs in emerging economies across Asia, Africa, and South America, as well as the provision of government subsidies for chip production in various other nations.<sup>64</sup> Additionally, the formidable cost structure associated with conducting business in the U.S. has played a contributory role.<sup>65</sup>

The CHIPS Act is intended to mitigate these challenges by investing in domestic semiconductor manufacturing research, development, and production.<sup>66</sup> It also provides funding for workforce development programs to train workers for the semiconductor industry.<sup>67</sup> The Act is a significant piece of legislation that has the potential to bolster U.S. semiconductor manufacturing competitiveness, reduce reliance on foreign chipmakers, and create jobs.<sup>68</sup> It is also a sign of the growing bipartisan consensus on the importance of investing in science and technology.<sup>69</sup> It follows in the footsteps of previous legislations like the Semiconductor Chip Protection Act (SCPA) of 1984, which focused on intellectual property protections for chip designs.<sup>70</sup> While the SCPA addressed

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59. *Id.* (discussing the role of chips in a variety of products).

60. *See SMIC Spent \$1.2 Billion to Order Lithography Machines, and After Adding 28nm Three Times, ASML Finally Heard the News*, iMEDIA (Oct. 1, 2023), <https://min.news/en/economy/4a2464956dbdc48315f7a46143bd3546.html> [<https://perma.cc/D4TK-TDZR>] (discussing the influence of SMIC and China generally in the semiconductor supply chain).

61. *Id.*

62. *See generally id.* (discussing China's influence in the creation of semiconductor chips).

63. PRESIDENT'S COUNCIL, *supra* note 39.

64. *See The Decline in Semiconductor Manufacturing in the United States*, CTR. FOR PUB. POL'Y INNOVATION (Sept. 2022), <https://www.cppionline.org/wp-content/uploads/2017/07/The-Divide-of-Semiconductor-Manufacturing.pdf> [<https://perma.cc/Y82F-MFNN>] (discussing the decline in semiconductor manufacturing in the US).

65. *See* PRESIDENT'S COUNCIL, *supra* note 39 (discussing the present issues associated with the chip manufacturing business in the US).

66. *See id.* (discussing the goals of the CHIPS act).

67. *Fact Sheet: Two Years after the CHIPS and Science Act, Biden-Harris Administration Celebrates Historic Achievements in Bringing Semiconductor Supply Chains Home, Creating Jobs, Supporting Innovation, and Protecting National Security*, THE WHITE HOUSE (Aug. 9, 2024), <https://www.whitehouse.gov/briefing-room/statements-releases/2024/08/09/fact-sheet-two-years-after-the-chips-and-science-act-biden> [<https://perma.cc/6JRY-BD8C>].

68. Anthony B. Kim & Dustin Carmack, *CHIPS Act Spending Is Making America Less Free*, THE HERITAGE FOUND. (Aug. 5, 2022), <https://www.heritage.org/budget-and-spending/commentary/chips-act-spending-making-america-less-free> [<https://perma.cc/B8U5-P5UD>].

69. *See id.* (discussing the passage of the CHIPS act with the help of both major US political parties).

70. *See* KIMIA ZAMIRI AZAR ET AL., UNDERSTANDING LOGIC LOCKING 47–62 (Springer International Publishing 2023) (discussing the SCPA of 1984 and the history of IP protection).

legal aspects of semiconductor innovation, the CHIPS Act emphasizes manufacturing and supply chain resilience.<sup>71</sup> Congress's understanding of semiconductor technology has evolved considerably.<sup>72</sup> Earlier legislation focused on IP and competition, whereas the CHIPS Act reflects a deeper grasp of the industry's strategic importance, integrating economic, technological, and security considerations.<sup>73</sup> This shift illustrates a broader recognition of semiconductors as foundational to modern technology and national security.<sup>74</sup> Initially, legislative efforts like the SCPA focused narrowly on intellectual property concerns.<sup>75</sup> However, with the CHIPS Act, Congress demonstrated a deeper grasp of the complexities and strategic importance of semiconductor manufacturing, recognizing its critical role in national security, economic competitiveness, and technological leadership.<sup>76</sup> This informed understanding led to broad bipartisan support, reflecting an awareness of the need for robust domestic production capabilities in response to global supply chain challenges and geopolitical competition.<sup>77</sup>

The CHIPS Act was the culmination of a bipartisan effort that began in late 2020.<sup>78</sup> In December 2020, the Senate passed the Endless Frontier Act, which provided \$190 billion for scientific research, including semiconductor research.<sup>79</sup> In February 2021, the House passed the CHIPS for America Act, which provided \$39 billion for semiconductor manufacturing subsidies.<sup>80</sup> The two bills were merged into the CHIPS Act, passed by the House in July 2022 and the Senate in August 2022.<sup>81</sup> President Biden signed The Act into law on August 9, 2022.<sup>82</sup>

### C. *Specific Allocation of Federal Subsidies for Supporting Chip Manufacturing in the U.S.*

The CHIPS Act allocates a specific amount of about \$53 billion for the American semiconductor business, which can be broadly divided into two different streams of subsidies for helping chip manufacturing in the U.S. as well as research development and workforce training.<sup>83</sup>

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71. Joshua Becker, *The Semiconductor Industry's Need for Better Negotiation to Combat China's Rise*, 24 CARDOZO J. CONFLICT RESOL. 167, 169–171 (2022).

72. KAREN M. SUTTER ET AL., CONG. RSCH. SERV., SEMICONDUCTORS AND THE CHIPS ACT: THE GLOBAL CONTEXT 1–3 (2023).

73. *Id.* (discussing the evolution of Congress's legislation on semiconductor technology).

74. *See id.* (discussing the shift in legislation between the SCPA and the CHIPS act).

75. Robert W. Kastenmeier & Michael J. Remington, *The Semiconductor Chip Protection Act of 1984: A Swamp or Firm Ground*, 70 MINN. L. REV. 417, 421 (1986).

76. *See* JOHN F. SARGENT JR. ET AL., CONG. RSCH. SERV., FREQUENTLY ASKED QUESTIONS: CHIPS ACT OF 2022 PROVISIONS AND IMPLEMENTATION 1 (Apr. 2023). (discussing the strategic and technological importance of semiconductors).

77. *See* Kim & Carmack, *supra* note 68 (discussing the bipartisan passing of the CHIPS act).

78. *Id.*

79. United States Innovation and Competition Act of 2021, S.1260, 117th Cong. (2021).

80. CHIPS for America Act, H.R. 7178, 116th Cong. (2020).

81. CHIPS and Science Act, H.R. 4346, 117th Cong. (2022).

82. *Id.*

83. *See* THE WHITE HOUSE, *supra* note 15.

1. *Direct Subsidy and Tax Break for Chip Manufacturing in the U.S.*

\$39 billion in direct subsidies for chip manufacturing on U.S. soil will be used to support the construction and expansion of semiconductor manufacturing facilities in the U.S.<sup>84</sup> There is a specific allocation of \$2 billion intended for the production of mature semiconductors essential for military applications, as well as for the automotive and manufacturing sectors.<sup>85</sup> In addition, 25% investment tax credits for costs of manufacturing equipment: this tax break will make it more affordable for companies to invest in new semiconductor manufacturing equipment.<sup>86</sup>

2. *Direct Subsidy for Research Development and Workforce Training*

Based on the CHIPS Act, a total sum of \$13.2 billion for semiconductor research and workforce training will be used to support semiconductor research and development at universities and national laboratories, as well as to train workers for the semiconductor industry.<sup>87</sup> \$10 billion will be allocated to invest in regional innovation and technology hubs across the country.<sup>88</sup> These hubs will bring together state and local governments, institutes of higher education, labor unions, businesses, and community-based organizations to create regional partnerships to develop technology, innovation, and manufacturing sectors.<sup>89</sup> \$2.8 billion will be used to support STEM education programs in schools and colleges to strengthen STEM education.<sup>90</sup> The Act also assigns funds to support programs that promote diversity and inclusion in the semiconductor industry.<sup>91</sup>

The CHIPS Act's broader, real-life implications across America are substantial, as it drives domestic semiconductor manufacturing, secures supply chains, and enhances national security.<sup>92</sup> By funding new facilities and upgrading existing ones, the Act promotes job creation in various regions,

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84. *Id.*

85. *The CHIPS Act: What It Means for the Semiconductor Ecosystem*, PwC, <https://www.pwc.com/us/en/library/chips-act.html> [<https://perma.cc/CUE4-NZPR>] (last visited Sep. 14, 2024).

86. See THE WHITE HOUSE, *supra* note 15 (“[The CHIPS Act] provides a 25 percent investment tax credit for capital expenses for manufacturing of semiconductors and related equipment.”).

87. *Id.*

88. BRIAN DARMODY, *THE GEOGRAPHY OF TECHNOLOGY, SCIENCE, AND INNOVATION UNDER THE CHIPS AND SCIENCE ACT*, 4 (Ass’n of Univ. Rsch. Parks eds.).

89. THE WHITE HOUSE, *supra* note 15.

90. See Martha Ross & Mark Muro, *How Federal, State, and Local Leaders Can Leverage the CHIPS and Science Act as a Landmark Workforce Opportunity*, BROOKINGS (Jan. 4, 2024), <https://www.brookings.edu/articles/how-federal-state-and-local-leaders-can-leverage-the-chips-and-science-act-as-a-landmark-workforce-opportunity/> [<https://perma.cc/2EK5-UPDB>] (“Standalone education and training programs [under the CHIPS Act] total \$2.8 billion in authorized spending.”).

91. THE WHITE HOUSE, *supra* note 15.

92. See William Alan Reinsch & Thibault Denamiel, *The CHIPS and Science Act Guardrails’ Implications for the U.S. Trade Agenda*, CNTR. STRATEGIC & INT’L STUD. (Apr. 13, 2023), <https://www.csis.org/analysis/chips-and-science-act-guardrails-implications-us-trade-agenda> [<https://perma.cc/KK6P-KGUN>] (stating that the CHIPS and Science Act invests in the U.S. semiconductor industry’s development and aids national security).

revitalizing local economies and reducing reliance on foreign suppliers.<sup>93</sup> A good example can be found in the case of emerging technologies like Gallium Nitride (GaN), known for their efficiency in power handling, are pivotal in the semiconductor industry's evolution, offering significant economic opportunities.<sup>94</sup> The CHIPS Act supports this resurgence by providing incentives for companies to innovate and expand.<sup>95</sup> For example, a semiconductor plant in Vermont, previously struggling, has received funding through the CHIPS Act to modernize its facilities, leading to job creation and revitalization of the local economy.<sup>96</sup> The focus on GaN and similar technologies underlines the Act's role in fostering advanced manufacturing,<sup>97</sup> ensuring that the U.S. remains competitive in the global tech landscape while creating high-quality jobs and driving economic growth.<sup>98</sup> Overall, the CHIPS Act aims to strengthen America's technological leadership, ensuring long-term economic stability and global competitiveness.<sup>99</sup>

### 3. *Job Creation and Protection of Supplies of Chips*

The CHIPS Act is also expected to create jobs in the U.S.<sup>100</sup> The semiconductor industry is high-wage, and the CHIPS Act is expected to create thousands of new jobs in chip manufacturing, research, and development.<sup>101</sup> In addition to these economic benefits, the CHIPS Act is also expected to strengthen U.S. national security.<sup>102</sup> Semiconductors are essential components in a wide range of military and civilian systems, and the U.S. needs to have a

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93. Mark Muro, *Can the CHIPS Act Heal the Nation's Economic Divides?*, BROOKINGS (Aug. 2, 2022), <https://www.brookings.edu/articles/can-the-chips-act-heal-the-nations-economic-divides/> [<https://perma.cc/34Y9-AFYV>].

94. TONGKAI LIU, ANALYSIS ON THE APPLICATION, DEVELOPMENT, AND FUTURE PROSPECTS OF GALLIUM NITRIDE (GAN) I (2020).

95. See, e.g., *Biden-Harris Administration Announces Preliminary Terms with GlobalFoundries to Strengthen Domestic Legacy Chip Supply for U.S. Auto and Defense Industries*, U.S. DEP'T COM. (Feb. 19, 2024), <https://www.commerce.gov/news/press-releases/2024/02/biden-harris-administration-announces-preliminary-terms-globalfoundries> [<https://perma.cc/PPV5-MTCX>] (noting an example of CHIPS Act funding going to a GaN manufacturing facility).

96. *Id.*

97. Sujai Shivakumar et al., *Gallium Nitride: A Strategic Opportunity for the Semiconductor Industry*, CNTR. STRATEGIC & INT'L STUD. (May 20, 2024), <https://www.csis.org/analysis/gallium-nitride-strategic-opportunity-semiconductor-industry> [<https://perma.cc/HZN8-Q3JE>].

98. *Id.*

99. THE WHITE HOUSE, *supra* note 15.

100. See *Two Years Later: Funding from CHIPS and Science Act Creating Quality Jobs, Growing Local Economies, and Bringing Semiconductor Manufacturing back to America*, U.S. DEP'T COM. (Aug. 9, 2024), <https://www.commerce.gov/news/blog/2024/08/two-years-later-funding-chips-and-science-act-creating-quality-jobs-growing-local> [<https://perma.cc/86NU-Q53C>] (stating that the CHIPS Act is expected to bring over 115,000 jobs across the country).

101. Marta Campabadal Graus, *Is Biden Right That You Don't Need a College Degree to Make \$110,000 in the Semiconductor Field?*, AUSTIN AMERICAN-STATESMAN (Apr. 18, 2024, 5:04 AM), <https://www.statesman.com/story/news/politics/politifact/2024/04/18/semiconductor-industry-employees-need-college-degrees-six-figures-contrary-to-biden/73342681007/> [<https://perma.cc/M3ER-6JFW>] (commenting on fact check ruling on Politifact.com).

102. THE WHITE HOUSE, *supra* note 15.

secure domestic supply of semiconductors.<sup>103</sup> The CHIPS Act will help reduce the U.S. reliance on foreign-made semiconductors and make the U.S. more resilient to supply chain disruptions.<sup>104</sup>

The CHIPS Act is a significant investment in the U.S. semiconductor industry and is expected to positively impact chip manufacturing in the U.S.<sup>105</sup> The Act is expected to attract new investment, create jobs, reduce reliance on foreign chips, and increase U.S. competitiveness in the global semiconductor market.<sup>106</sup>

#### D. Geographical Manufacturing Restrictions

The CHIPS Act provides a valuable opportunity for substantial progress in chip manufacturing within the U.S. However, it is crucial to acknowledge that these funding provisions come with a significant stipulation: manufacturing is required to occur exclusively on the soil of the U.S. and its allies.<sup>107</sup>

To leverage the benefits of the CHIPS Act, semiconductor companies ought to reevaluate their global strategy and concurrently strategize for the grant application, embark on digital transformation initiatives, manage capital projects effectively, and engage in prudent financial planning. Recipients of the funding are bound by the stipulation that they cannot expand semiconductor manufacturing operations in China or any other countries deemed as posing a threat to U.S. national security.<sup>108</sup> These subsidies serve as a buffer for semiconductor companies to elevate the skills and diversity of their workforce, positioning them on a trajectory toward enhanced competitiveness in chip manufacturing.<sup>109</sup>

These restrictions are subject to potential modification. The Act mandates a 10-year review period, led by the Secretary of Commerce in collaboration with the Secretary of Defense and Director of National Intelligence, in consultation with industry stakeholders.<sup>110</sup> This ensures alignment with current

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103. See Sujai Shivakumar & Charles Wessner, *Semiconductors and National Defense: What are the Stakes?*, CNTR. STRATEGIC & INT'L STUD. (June 8, 2022), <https://www.csis.org/analysis/semiconductors-and-national-defense-what-are-stakes> [<https://perma.cc/K7TW-53TN>] (“All major U.S. defense systems and platforms rely on semiconductors for their performance.”).

104. See Alexander Kersten et al., *A Look at the CHIPS-Related Portions of CHIPS+*, CNTR. STRATEGIC & INT'L STUD. (Aug. 9, 2022), <https://www.csis.org/analysis/look-chips-related-portions-chips> [<https://perma.cc/43B3-5BG9>] (“The provisions seek to lessen U.S. reliance on foreign manufacturing sources . . .”).

105. *Id.*

106. *Id.*

107. See THE WHITE HOUSE, *supra* note 15 (explaining guardrails to ensure recipients of the CHIPS Act funds “do not build certain facilities in China and other countries of concern . . .”).

108. Sujai Shivakumar et al., “Guardrails” on CHIPS Act Funding to Restrict Investments in China May Restrict Participation in CHIPS Act Incentives, CNTR. STRATEGIC & INT'L STUD. (Nov. 7, 2023), <https://www.csis.org/blogs/perspectives-innovation/guardrails-chips-act-funding-restrict-investments-china-may-restrict> [<https://perma.cc/8BQV-A5S3>].

109. See Ross & Muro, *supra* note 90 (“The CHIPS and Science Act directs the investment . . . to . . . roadly support . . . workforce development.”); see also THE WHITE HOUSE, *supra* note 15 (“The legislation authorizes investments to expand the geographic and institutional diversity of research institutions and the students and researchers they serve . . .”).

110. 15 C.F.R. § 231.202 (2024).

semiconductor technology and U.S. export control regulations.<sup>111</sup> Companies must conduct a thorough assessment to weigh the benefits of federal funding against the constraints of geographical manufacturing restrictions.<sup>112</sup> This requires evaluating the strategic implications and long-term viability of pursuing funding under these conditions.<sup>113</sup>

By allowing for the specification of “foreign entities of concern,” the Act addresses concerns about intellectual property protection, supply chain integrity, and national security.<sup>114</sup> These restrictions aim to safeguard sensitive technologies from unauthorized access or exploitation by foreign entities.<sup>115</sup> Additionally, they mitigate risks tied to potential geopolitical tensions stemming from concentrated semiconductor production.<sup>116</sup> However, these restrictions pose complex economic and operational challenges for semiconductor companies.<sup>117</sup> This includes reevaluating partnerships and supply chains, potentially requiring significant restructuring.<sup>118</sup> Companies may also need to diversify manufacturing beyond restricted regions to remain competitive and comply with the Act.<sup>119</sup>

### *E. Implications and Influences: The China Factor*

The CHIPS Act addresses concerns over the reliance of the U.S. on foreign-made semiconductors, particularly China’s substantial role in producing over 15% of the world’s semiconductors.<sup>120</sup> China aims for semiconductor self-

111. See *Follow the Money: The CHIPS and Science Act’s (Limited) Outbound Review Mechanism*, DECHERT (Apr. 13, 2023), <https://www.dechert.com/knowledge/onpoint/2023/4/follow-the-money--the-chips-and-science-act-s--limited--outbound.html> [<https://perma.cc/KJ6K-864H>] (“[T]he outbound review mechanism in the CHIPS Act will require funding recipients to balance the benefits of funding against the restrictions on certain foreign investments . . . .”); see also *U.S. Expands China-Related Export Controls Regarding Semiconductors and Semiconductor Manufacturing Equipment*, ORRICK (Oct. 26, 2023), <https://www.orrick.com/en/Insights/2023/10/US-Expands-China-Related-Export-Controls-Regarding-Semiconductor-Manufacturing-Equipment> [<https://perma.cc/EA5U-79EM>] (describing revised export control regulations related to the export of semiconductors to China).

112. DECHERT, *supra* note 111.

113. See Shivakumar et al., *supra* note 108 (describing the “guardrails” [of the CHIPS Act] as potentially having a counterproductive effect on the global chipmaking and semiconductor supply chain).

114. See *id.* (defining “foreign entities of concern”).

115. *Id.*

116. See Peters, *supra* note 16, at 1644 (2022) (stating that the CHIPS Act will reduce US dependence on concentrated foreign supply chains in the semiconductor industry).

117. See Shivakumar et al., *supra* note 108 (describing the “guardrails” as potentially having a counterproductive effect on the global chipmaking and semiconductor supply chain).

118. See *id.* (discussing companies that have stated that the restrictions imposed by the CHIPS Act can force them to make difficult decisions about business transactions and participation internationally).

119. See Vishnu Kannan & Jacob Feldgoise, *After the CHIPS Act: The Limits of Reshoring and Next Steps for U.S. Semiconductor Policy*, CARNEGIE (Nov. 22, 2022), <https://carnegieendowment.org/research/2022/11/after-the-chips-act-the-limits-of-reshoring-and-next-steps-for-us-semiconductor-policy?lang=en> [<https://perma.cc/NA7Q-A4Z2>] (discussing the importance of chip manufacturers diversifying in the event of economic shocks in certain global regions).

120. *China’s Share of Global Chip Sales Now Surpasses Taiwan’s, Closing in on Europe’s and Japan’s*, SEMICONDUCTOR INDUS. ASS’N (Jan. 10, 2022), <https://www.semiconductors.org/chinas-share-of-global-chip-sales-now-surpasses-taiwan-closing-in-on-europe-and-japan/> [<https://perma.cc/BU3S-4BNE>].

sufficiency by 2030.<sup>121</sup> The Act counters China's growing dominance, safeguards the U.S. technological edge, and is anticipated to bolster the economy and job creation.<sup>122</sup>

First, the Act attempts to diminish U.S. dependency on foreign-made semiconductors, enhancing resilience against supply chain disruptions and bolstering control over critical technology supply.<sup>123</sup> Second, it amplifies investment in domestic semiconductor manufacturing with \$52 billion in subsidies, attracting new investments and job opportunities.<sup>124</sup> Third, the Act bolsters technological competitiveness through \$170 billion in research funding over five years, ensuring U.S. leadership over China and other nations.<sup>125</sup> However, the Act heightens tensions with China, posing a threat to their semiconductor industry and broader technological self-sufficiency goals.<sup>126</sup>

Beyond the stated implications, the Act fosters heightened competition among semiconductor manufacturers, potentially yielding lower prices and increased innovation.<sup>127</sup> It also prompts diversification in the global semiconductor supply chain, reducing reliance on single sources and enhancing industry resilience to disruptions.<sup>128</sup> For example, the CHIPS Act's impact on a small semiconductor plant in Vermont highlights how the legislation is revitalizing local economies.<sup>129</sup> This plant, previously considered outdated,

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121. See James Andrew Lewis, *China's Pursuit of Semiconductor Independence*, CNTR. STRATEGIC & INT'L STUD. (Feb. 27, 2019), <https://www.csis.org/analysis/chinas-pursuit-semiconductor-independence> [<https://perma.cc/7HA3-K7U3>] ("China's State Council set the goal of becoming a global leader in all segments of the semiconductor industry by 2030.").

122. THE WHITE HOUSE, *supra* note 15.

123. See John Neuffer, *Two Years After CHIPS Enactment, Here's how to Sustain America's Budding Semiconductor Resurgence*, SEMICONDUCTOR INDUS. ASS'N (Aug. 8, 2024, 12:00 PM), <https://www.semiconductors.org/two-years-after-chips-enactment-heres-how-to-sustain-americas-budding-semiconductor-resurgence/> [<https://perma.cc/P4JA-RHCF>] ("Achieving these projections would make the U.S. less vulnerable to supply chain disruptions . . .").

124. THE WHITE HOUSE, *supra* note 15.

125. Katie Lobosco, *Here's What's in the Bipartisan Semiconductor Chip Manufacturing Package*, POLITICS, CNN (Aug. 9, 2022, 11:31 AM), <https://www.cnn.com/2022/08/09/politics/chips-semiconductor-manufacturing-science-act/index.html> [<https://perma.cc/LXC8-WN9A>].

126. See Zhou, *supra* note 21, at 407 ("Moreover, the Chip and Science Act contains provisions implying competition with China. It states that companies receiving subsidies cannot expand their semiconductor factories in China within a decade.").

127. See Yadong Luo & Ari Van Assche, *The Rise of Techno-Geopolitical Uncertainty: Implications of the United States CHIPS and Science Act*, 54 J. INT'L BUS. STUD. 1423, 1428 (2023) ("While big players that build US manufacturing operations are the ones who will gain the most from the Act, there is the belief among many that smaller companies can be indirect benefactors . . . . There will certainly be a trickle-down effect where component makers see an increase in orders as the giant manufacturers build out."); see also Nick Frasse, *Fabless Semiconductor Companies: Winners in the CHIPS Act Era*, VANECK (Aug. 28, 2024), <https://www.vaneck.com/us/en/blogs/thematic-investing/fabless-semiconductor-companies-winners-in-the-chips-act-era/> [[perma.cc/Y5KA-LZT2](https://perma.cc/Y5KA-LZT2)] ("The CHIPS Act is revolutionizing the semiconductor industry, giving fabless chip designers lower production costs, improved technology access, and greater flexibility, driving innovation and competitiveness.").

128. See Luo & Assche, *supra* note 127, at 1435 ("Resilience may be emphasized for [multinational enterprises] whose global value chain for semiconductor businesses is more internationally diversified.")

129. See Henry Epp, *With CHIPS Act Money, the Biden Administration Bets an Old Plant Can Make New Chips*, MARKETPLACE (Mar. 26, 2024), <https://www.marketplace.org/2024/03/26/with-chips-act-money-the-biden-administration-bets-an-old-plant-can-make-new-chips/> [<https://perma.cc/KD86-YJ2L>] (stating that "[a] previous \$30 million federal grant helped GlobalFoundries carry out a successful pilot making gallium nitride chips," and that at least "400 construction jobs" are expected to be created); see also the discussion provided in

received a boost from the Act, enabling it to produce advanced chips and create new jobs in a rural area.<sup>130</sup> Additionally, emerging technologies like Gallium Nitride (GaN), known for handling higher power levels, are making a comeback.<sup>131</sup> This resurgence, fueled by legislative support, is leading to innovative applications and expanding job opportunities in various regions.<sup>132</sup> By including these stories,<sup>133</sup> the article can showcase the tangible benefits of these policies, illustrating their far-reaching effects on everyday lives and local communities.

The CHIPS Act is also set to stimulate competition among semiconductor manufacturers, potentially leading to lower prices and increased innovation.<sup>134</sup> It is also expected to prompt diversification in the global semiconductor supply chain, reducing reliance on single sources and thus enhancing industry resilience.<sup>135</sup> Nevertheless, the Act faces challenges like a shortage of skilled workers and rising manufacturing costs.<sup>136</sup>

While the CHIPS Act is poised to attract investment and lead to the construction of new fabrication plants in the U.S., its full impact will unfold gradually.<sup>137</sup> It is essential to acknowledge that this Act is not a panacea, and ongoing challenges persist.<sup>138</sup> Nevertheless, its multifaceted approach is anticipated to yield positive outcomes, including reduced reliance on foreign-made semiconductors, increased competition, and diversified global supply

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Breándaín Ó hUallacháin, *Restructuring the American Semiconductor Industry: Vertical Integration of Design Houses and Wafer Fabricators*, 87 ANNALS ASS'N AM. GEOGRAPHERS 217, 217 (1997) (“The semiconductor industry . . . and conjecture on the structure of the industry has become the cornerstone of generalizations about the direction of regional development.”).

130. See Epp, *supra* note 129 (stating that “[a] previous \$30 million federal grant helped GlobalFoundries carry out a successful pilot making gallium nitride chips,” and that at least “400 construction jobs” is expected to be created).

131. Syed Mudassir & Jan Muhammad, *A Review of Gallium Nitride (GaN) Based Devices for High Power and High Frequency Applications*, 4 J. APPLIED & EMERGING SCI. 141, 142 (2016) (For example, “in case of GaN [the JFoM] is 760 times higher than the Si,” and “in case of GaN [the KFoM] is 1.6 times higher than Si”).

132. Weixiang Xiong, *Advanced Electronics: The Emergence, Evolution, and Future of Gallium Nitride Technology*, 5 TRANSACTIONS ON COMPUT. SCI. & INTELLIGENT SYSS. RSCH. 693, 697 (2024).

133. See *supra* text accompanying note 129; see Mudassir & Muhammad, *supra* text accompanying note 131; see also Xiong, *supra* text accompanying note 132.

134. Luo & Assche, *supra* note 127, at 1428.

135. *Ibid.*

136. See *Chipping Away: Assessing and Addressing the Labor Market Gap Facing the U.S. Semiconductor Industry*, SEMICONDUCTOR INDUS. ASS'N, <https://www.semiconductors.org/chipping-away-assessing-and-addressing-the-labor-market-gap-facing-the-u-s-semiconductor-industry/> [<https://perma.cc/3JDK-794C>] (last visited Sept. 12, 2024) (discussing the growth of the semiconductor’s workforce and that the new jobs risk going unfilled at current degree completion rates); see also, Dylan Sloan, *CHIPS Act Faces Talent Shortage Despite \$500 Billion Investment: ‘We Have to Make Semiconductor Manufacturing Sexy,’* FORTUNE (Jun. 9, 2024, 4:00 AM), <https://fortune.com/2024/06/09/chips-act-talent-workforce-shortage-tsmc-semiconductor-manufacturing-fabs-intel/> [[perma.cc/NFC4-3E3V](https://perma.cc/NFC4-3E3V)] (“But [TSMC is] running to the same problem as many of its competitors—a severe talent shortage that government officials and educators are hard at work trying to reverse.”).

137. See THE WHITE HOUSE, *supra* note 15 (“Spurred by the passage of the CHIPS and Science Act of 2022, this week, companies have announced nearly \$50 billion in additional investments in American semiconductor manufacturing . . . .”); see also Badlam et al., *supra* note 44 (“Seventy semiconductor fabrication plants (known as fabs) are currently under construction in Arizona and Texas; dozens more have been announced or are already under way in other states.”).

138. See, e.g., Peter Clarke, *China’s Synchrotron EUV Lithography Light Source is No Sanctions Buster*, EENews (Sept. 25, 2023), <https://www.eenewseurope.com/en/chinas-synchrotron-euv-litho-light-source-is-no-sanctions-buster/> [<https://perma.cc/AB9S-NE4Q>] (introducing that Chinese researchers are exploring “the use of an electron accelerator as a light source for lithography”).

chains, ultimately influencing downstream economic activities and employment opportunities.<sup>139</sup>

#### F. *Limitations and Potential Shortcomings*

The CHIPS Act is a landmark legislation expected to significantly impact the U.S. semiconductor industry and scientific research.<sup>140</sup> However, the Act also has some limitations and potential shortcomings.

One limitation of the CHIPS Act is that it is a long-term investment.<sup>141</sup> It will take several years for the new chip fabrication plants to be built and for the research and development investments to produce results.<sup>142</sup> In the meantime, the U.S. semiconductor supply chain will continue to be vulnerable to disruptions.<sup>143</sup> Another limitation of the Act is that it does not address all the challenges facing the U.S. semiconductor industry.<sup>144</sup> For example, the Act does not address the issue of labor shortages in the semiconductor industry.<sup>145</sup> Additionally, the Act does not address the issue of intellectual property theft, which is a major concern for U.S. semiconductor companies.<sup>146</sup>

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139. See generally THE WHITE HOUSE, *supra* note 15 (stating the CHIPS and Science Act will “[p]romote U.S. innovation in wireless supply chain. . . . [a]dvance U.S. global leadership in the technologies of the future. . . . [and] [c]atalyze regional economic growth and development.”); see also Luo & Assche, *supra* note 128, at 1428.

140. See, e.g., Vivien Bui, *The CHIPS and Science Act: A Game-Changer in its First Year*, DEP’T ENERGY (Aug. 10, 2023), <https://www.energy.gov/articles/chips-and-science-act-game-changer-its-first-year> [perma.cc/A298-J7E2] (“This groundbreaking legislation, aimed at boosting the semiconductor industry and advancing scientific endeavors, has set the stage for innovation and progress. Here are four ways it’s been changing the game in its first year.”).

141. See, e.g., Jared Mondschein, *The Chips Act Alone Won’t Secure U.S. Semiconductor Supply Chains*, RAND (Oct. 12, 2022), <https://www.rand.org/pubs/commentary/2022/10/the-chips-act-alone-wont-secure-us-semiconductor-supply.html> [https://perma.cc/LJ3G-SU9V] (“But executing on these ambitions could take some time: to staff federal program offices, to solicit proposals from industry and academia, to mature a sufficient workforce, and to construct new fabrication facilities.”); see also Kannan & Feldgoise, *supra* note 119 (“The CHIPS Act was only the first step of what will likely be a long journey.”).

142. *Id.*; see also Stephanie Hughes, *What Does It Take for Chip Manufacturers to Get a New Plant Up and Running?*, MARKETPLACE (Aug. 23, 2022), <https://www.marketplace.org/2022/08/23/what-does-it-take-for-chip-manufacturers-to-get-a-new-plant-up-and-running/> [https://perma.cc/F7PE-SNWV] (“[E]ach chip factory takes a minimum of \$10 billion and five years to build.”).

143. See Mondschein, *supra* note 141 (“Without addressing near-term resilience concerns, the U.S. government, U.S. military, and the general public remain vulnerable to semiconductor supply chain issues.”); see also David Simchi-Levi et al., *Fixing the U.S. Semiconductor Supply Chain*, HARV. BUS. REV. (Oct. 25, 2022), <https://hbr.org/2022/10/fixing-the-u-s-semiconductor-supply-chain> [perma.cc/Y6SG-M53Y] (“A study . . . in Japan, highlighted how vulnerable the semiconductor supply chain is to disruptions. . . . a short disruption of a semiconductor fabrication facility, or “fab,” in Taiwan for 10 days, could cause a flurry of additional disruptions across the entire supply chain that would last almost a year.”).

144. Sloan, *supra* note 136 (arguing that CHIPS Act faces talent shortage despite \$500 billion investment).

145. *Id.*

146. See *Avoiding Semiconductor Intellectual Property Theft*, AALBUN, <https://www.aalbun.com/blog/avoiding-semiconductor-intellectual-property-theft> [https://perma.cc/MGL3-P4HZ] (last visited Sept. 15, 2024) (“Because the semiconductor industry is so innovative, regularly vying with pharmaceuticals and biotech for this title of most innovative, the value of the intellectual property (IP) has gone up.”); see also Alan O. Sykes & Sharon Driscoll, *Stanford’s Al Sykes on the \$280 Billion Chips and Science Act, Government Intervention and Trade*, SLS BLOGS (Aug. 2, 2022), <https://law.stanford.edu/2022/08/02/stanfords-al-sykes-on-the-280-billion-chips-and-science-act-government-intervention-and-trade/> [perma.cc/8HJ4-PV8B] (“The legislation does not address alleged intellectual property theft by China, preclude joint ventures with Chinese companies or introduce any new limits on U.S. exports to China or Chinese investment in the United States.”).

In addition to these limitations, the CHIPS Act also has some potential shortcomings. One potential shortcoming is that the Act could lead to increased government intervention in the semiconductor industry.<sup>147</sup> This could stifle innovation and make the industry less competitive.<sup>148</sup> Another potential shortcoming is that the Act could lead to trade tensions with China.<sup>149</sup> China is a major player in the semiconductor industry, and it is investing heavily in its domestic chip industry.<sup>150</sup> China may view the CHIPS Act as a threat to its semiconductor industry and its broader goal of becoming self-sufficient in critical technologies.<sup>151</sup>

The CHIPS Act is a long-term investment and cannot address all of the industry's challenges.<sup>152</sup> Additionally, the Act could lead to increased government intervention in the semiconductor industry and to trade tensions with China.<sup>153</sup>

### III. OVERVIEW OF THE EUROPEAN CHIPS ACT OF 2023

Similar to the CHIPS Act in the U.S., the European Chips Act of 2023 (the EU Chips Act) is a pivotal legislative measure aimed at bolstering the EU's semiconductor ecosystem and diminishing reliance on external suppliers.<sup>154</sup> Anticipated repercussions encompass substantial effects on the European and global semiconductor markets, as well as broader impacts on the European economy and society.<sup>155</sup>

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147. See George Calhoun, *Semiconductors—The CHIPS Act: What It Is (Part 1)*, FORBES (Feb. 25, 2023, 12:44 pm EST), <https://www.forbes.com/sites/georgecalhoun/2021/11/23/semiconductors--the-chips-act-why-it-is-what-it-is-part-1/> [perma.cc/7TV4-38H9] (“[The CHIPS Act] may become the biggest government intervention of its kind ever.”).

148. David Sacks & Seaton Huang, *Onshoring Semiconductor Production: National Security Versus Economic Efficiency*, COUNS. ON FOREIGN REL. (Apr. 17, 2024, 1:52 PM), <https://www.cfr.org/article/onshoring-semiconductor-production-national-security-versus-economic-efficiency> [perma.cc/6YAK-MRHJ], (“The push to build resiliency in the semiconductor industry could result in higher costs and less innovation.”).

149. See Luo & Assche, *supra* note 127, at 1430 (“China considers the Act (combined with other recent techno-nationalist policies) as an act of economic warfare against China’s semiconductor industry.”).

150. *Id.* at 1431 (“In 2020, China represented 53.7% of worldwide chip sales, or \$239.45 billion out of \$446.1 billion.”). See Laura He, *China Is Pumping Another \$47.5 Billion into Its Chip Industry*, CNN (May 28, 2024, 1:19 AM), <https://www.cnn.com/2024/05/27/tech/china-semiconductor-investment-fund-intl-hnk/index.html> [perma.cc/34DB-P6E2] (“China is doubling down on its plan to dominate advanced technologies of the future by setting up its largest-ever semiconductor state investment fund . . .”).

151. See Hufbauer & Hogan, *supra* note 19, at 19 (“While collective measures have inflicted considerable short-term pain on China, causing a sharp drop in the fortunes of its high-tech firms, China will respond by redoubling its self-sufficiency programs.”).

152. See *infra* Part II.F (discussing the challenges and issues the Act does not address); see also Kannan & Feldgoise, *supra* note 119.

153. See *infra* Part II.F (discussing the possible increase in government intervention and the tensions with China); see also Calhoun, *supra* note 147.

154. See Dachs, *supra* note 23, at 1 (“The EU Chips Act is a new policy instrument that aims to increase Europe’s autonomy in the area of microchips.”); see also EUR. COMM’N, *supra* note 25 (“The European Chips Act will bolster Europe’s competitiveness and resilience in semiconductor technologies and applications, and help achieve both the digital and green transition.”).

155. Christian Guillemot et al., *Transparent Optical packet Switching: The European ACTS KEOPS Project Approach*, 16 J. OF LIGHTWAVE TECH. 2117, 2130 (1998) (“New design methodologies based on the Intellectual Property concept allows design reuse and reduced time to market, key considerations in the dynamic telecommunication world dominated by economics and fast responses to new system and service requests.”).

The Act facilitates increased domestic semiconductor production within the EU through a €43 billion allocation for research, development, and manufacturing.<sup>156</sup> This funding will support establishing and modernizing semiconductor manufacturing facilities and facilitate research endeavors.<sup>157</sup> Furthermore, the Act seeks to diversify the EU's semiconductor supply chain by promoting the development of design tools, software, and workforce training.<sup>158</sup> This approach aims to reduce dependency on foreign semiconductor suppliers.<sup>159</sup> In tandem, the Act institutes a new framework to fortify the security of the EU's semiconductor supply chain, enhancing its resilience to disruptions.<sup>160</sup>

While the EU Chips Act holds substantial promise for reshaping the European supply chain, its full effectiveness is contingent on ongoing implementation efforts.<sup>161</sup> Collaboration between the EU semiconductor industry, governments, and research institutions will be crucial in realizing the Act's ambitious objectives.<sup>162</sup> Acknowledging the complexities,<sup>163</sup> it is imperative to maintain a pragmatic perspective on the Act's challenges and the time required for its comprehensive realization.

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156. See EUROPEAN COMMISSION, *supra* note 154 (“In total, more than €43 billion of policy-driven investment will support the Chips Act until 2030, which will be broadly matched by long-term private investment.”).

157. Alexandre G. Verheyden et al., *The EU Commission Proposes a Chip Act to Confront Semiconductor Shortages and Strengthen Europe's Technological Leadership*, CONCURRENCES (Feb. 8, 2022), <https://www.concurrences.com/en/bulletin/news-issues/february-2022/the-eu-commission-proposes-a-chip-act-to-confront-semiconductor-shortages-and> [<https://perma.cc/X8AT-49GG>].

158. See EUROPEAN COMMISSION, *supra* note 154 (“The aim is to Strengthen Europe's research and technology leadership towards smaller and faster chips . . . Build and reinforce capacity to innovate in the design, manufacturing and packaging of advanced chips . . . Address the skills shortage, attract new talent and support the emergence of a skilled workforce.”).

159. See *id.* (“This will be achieved based on three pillars of action . . . A framework to incentivise public and private investments in manufacturing facilities will ensure the security of supply and resilience of the Union's semiconductor sector.”); see also Guillaume Ragonnaud, *The EU Chips Act: Securing Europe's Supply of Semiconductors*, EU LEGIS. IN PROGRESS (June 2023), [https://www.europarl.europa.eu/RegData/etudes/BRIE/2022/733596/EPRS\\_BRI\(2022\)733596\\_EN.pdf](https://www.europarl.europa.eu/RegData/etudes/BRIE/2022/733596/EPRS_BRI(2022)733596_EN.pdf) [<https://perma.cc/RV6G-V35U>] (“Parliament stressed that the EU's lack of investment in technology has contributed to its current dependence on foreign suppliers. Parliament considers that the chips act represents an important step in limiting dependence on third countries . . .”).

160. See Ragonnaud, *supra* note 159, at 8 (“[The Commission] have introduced provisions specifying two general objectives for the chips act . . . and (ii) to improve the functioning of the single market, by setting up a uniform legal framework to improve the EU resilience and security of supply of chip technologies.”).

161. See Hancké & Calvo, *supra* note 27, at 590 (For example, the Act has a goal “of increasing semiconductor production from the current 10% of global supply to 20% by 2030. Because the global industry is expected to double in size by that year, this would mean quadrupling current production capacity—a huge challenge . . .”); see also *European Chips Act—Questions and Answers*, EUR. COMM'N (Nov. 29, 2023), [https://ec.europa.eu/commission/presscorner/detail/en/qanda\\_23\\_4519](https://ec.europa.eu/commission/presscorner/detail/en/qanda_23_4519) [<https://perma.cc/4JK5-9E7X>] (“The Chips Act is a unique opportunity for Europe to act jointly across all Member States, to the benefit of the whole Union.”).

162. See generally Dachs, *supra* note 23, at 2–6 (describing the Act's goals as “ambitious” and discussing the Act's structure and critiques).

163. *Ibid.*

A. *The European Chips Act's Provisions and Existing Industry Trends*

The EU Chips Act aims to strengthen the EU's semiconductor ecosystem and reduce its dependence on foreign suppliers.<sup>164</sup> The European Parliament and the Council of the EU adopted the Act on July 25, 2023, and entered into force on September 21, 2023.<sup>165</sup>

The EU Chips Act has five main objectives:<sup>166</sup>

1. To strengthen the EU's research and technological research.
2. To build and reinforce the EU's capacity to innovate in the design, manufacturing and packaging of advanced chips.
3. To increase the EU's global semiconductor market share to 20% and put an adequate framework to increase production by 2030.
4. To create new jobs and economic growth in the EU semiconductor sector.
5. To develop an in-depth understanding of global semiconductor supply chains.

The EU Chips Act is a strategic initiative aimed at fortifying the continent's semiconductor supply chain, responding to recent global chip scarcities and the race to subsidize production in key regions.<sup>167</sup> This initiative, coupled with the EU's renewed industrial policy, prompted the European Commission to propose the Act in February 2022.<sup>168</sup>

The EU Chips Act is structured upon a tripartite framework endorsed by co-legislative bodies: the first pillar emphasizes technological prowess and innovation within the EU's semiconductor ecosystem; the second pillar focuses on enhancing the Union's supply chain security; and the third pillar establishes a vigilance mechanism and crisis mitigation framework.<sup>169</sup> In the event of supply exigencies, the Commission is empowered to enact three forms of emergency measures: soliciting information from companies, urging precedence to orders of crisis-essential products, and executing collective procurements on behalf of Member States.<sup>170</sup>

The EU Chips Act allocates €43 billion for semiconductor research, development, and manufacturing in the EU.<sup>171</sup> These funds will support critical initiatives like establishing new semiconductor manufacturing plants, upgrading

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164. *Id.* at 1 ("The EU Chips Act is a new policy instrument that aims to increase Europe's autonomy in the area of microchips."); *see also* Ragonnaud, *supra* note 159, at 1–2.

165. Emily Benson et al., *Transatlantic Cooperation on Semiconductors and AI in 2024*, CENT. FOR STRATEGIC & INT'L STUD. (Jan. 17, 2024), <https://www.csis.org/analysis/transatlantic-cooperation-semiconductors-and-ai-2024> [https://perma.cc/ZH9Q-NBGQ].

166. EUR. COMM'N, *supra* note 154.

167. *Id.*

168. Jenny Gesley, *European Union: Commission Proposes EU Chips Act to Achieve More Resilient Supply Chain for Semiconductors*, LIBR. CONG. (Mar. 2, 2022), <https://www.loc.gov/item/global-legal-monitor/2022-03-02/european-union-commission-proposes-eu-chips-act-to-achieve-more-resilient-supply-chain-for-semiconductors/> [https://perma.cc/SCQ7-J595].

169. Ragonnaud, *supra* note 159, at 1.

170. *Ibid.*

171. *See* EUR. COMM'N, *supra* note 154.

existing ones, investing in research and development, fostering new design tools and software, and training a proficient semiconductor workforce.<sup>172</sup>

This Act is poised to significantly impact the European semiconductor industry, with projections of up to 100,000 new jobs and €20 billion in additional GDP annually by 2030.<sup>173</sup> It is also expected to influence the global semiconductor market, intensifying competition and potentially leading to lower prices, benefitting consumers and businesses worldwide.<sup>174</sup>

The EU Chips Act is a resolute initiative to strengthen the EU's semiconductor ecosystem and reduce reliance on external suppliers.<sup>175</sup> It is anticipated to influence both European and global semiconductor markets substantially.<sup>176</sup>

### B. *Evaluation of the Act's Capacity to Address Current European Supply Chain Problems*

The attempt of the EU Chips Act to rectify current challenges within the European semiconductor supply chain<sup>177</sup> merits a critical evaluation. While establishing new semiconductor manufacturing facilities within the EU holds promise in reducing external dependence on semiconductor procurement, it is crucial to recognize the formidable and resource-intensive nature of such ventures, characterized by intricate complexities and prolonged gestation periods.<sup>178</sup> Modernizing existing semiconductor manufacturing plants constitutes a pivotal initiative to bolster the EU's indigenous semiconductor production capacity.<sup>179</sup> However, it is imperative to acknowledge that this endeavor entails considerable intricacies and financial outlays.

Investments in semiconductor research and development are indispensable for the EU to maintain technological preeminence in semiconductor design and manufacturing.<sup>180</sup> Stakeholders need to appreciate that the returns from these investments may materialize over an extended temporal horizon.<sup>181</sup> Moreover, creating advanced semiconductor design tools and software is critical for enabling the EU to conceive and produce cutting-edge semiconductors.<sup>182</sup> Acknowledging that such tools and software development are intricate and

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172. *Id.*

173. Karen Weisz et al., *The Global Semiconductor Talent Shortage*, DELOITTE, <https://www2.deloitte.com/us/en/pages/technology/articles/global-semiconductor-talent-shortage.html> [<https://perma.cc/96SE-JCV9>] (last visited Sept. 14, 2024).

174. See EUR. COMM'N, *supra* note 154 (writing that the EU Chips Act aims to “[p]ut in place a framework to increase production capacity [from 10%] to 20% of the global market by 2030”).

175. EU LEGIS. IN PROGRESS, *supra* note 159, at 6.

176. *Ibid.*

177. *Ibid.*

178. Andreas Bier, *Semiconductor Device Manufacturing Process, Challenges and Opportunities*, RENESAS (Dec. 6, 2023), <https://www.renesas.com/en/blogs/semiconductor-device-manufacturing-process-challenges-and-opportunities> [<https://perma.cc/A7U8-UCF5>] (providing that “[t]he semiconductor device manufacturing process faces several challenges, including cost, complexity, and yield, but also presents significant opportunities for innovation and growth”).

179. EUR. COMM'N, *supra* note 154.

180. *Id.*

181. *Id.*

182. *Id.*

fiscally demanding is paramount.<sup>183</sup> Nurturing a proficient workforce in semiconductor technology is foundational for the EU to ensure the sustenance and growth of its semiconductor industry.<sup>184</sup> However, it is important to recognize that the process of training new semiconductor professionals demands a substantial investment of time.<sup>185</sup>

While the EU Chips Act holds substantial promise for enhancing the European semiconductor supply chain, it is crucial to temper expectations with a realistic understanding of the time required for its full realization and subsequent impact.<sup>186</sup> Additionally, several supplementary factors are pertinent to the EU Chips Act's efficacy in addressing the prevailing dynamics within the European semiconductor supply chain.<sup>187</sup> Firstly, it is crucial to acknowledge the fiercely competitive nature of the global semiconductor market, where the EU will contend with formidable counterparts.<sup>188</sup> Moreover, it is imperative to recognize the intrinsically cyclical nature of the semiconductor industry and formulate policies to fortify its resilience.<sup>189</sup> Ensuring unfettered access to requisite capital for technological advancement and manufacturing expansion is also crucial, given the capital-intensive nature of the semiconductor industry.<sup>190</sup>

The EU Chips Act represents a commendable stride towards ameliorating present exigencies within the European semiconductor supply chain.<sup>191</sup> Nevertheless, it is essential to acknowledge and address the complex challenges ahead, including global competition, resilience against cyclical downturns, and robust access to capital for technological advancement and manufacturing expansion.<sup>192</sup>

### C. *Initializing the Semiconductor Supply Chain Alert System*

The European Commission has initiated a pilot initiative known as the Semiconductor Alert System, a component of the third pillar within the European Chips Act.<sup>193</sup> This system precedes the establishment of the European Semiconductor Board and is designed to enhance the preparedness and oversight of the European semiconductor supply network.<sup>194</sup> It enables semiconductor enterprises and their stakeholders to promptly communicate disruptions along the semiconductor value chain.<sup>195</sup> The objective is to accumulate requisite data

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183. *Id.*

184. Ragonnaud, *supra* note 159.

185. *Id.* at 6.

186. *Id.*

187. *Id.*

188. *Id.* at 3–4.

189. *Id.* at 9–10.

190. *Id.* at 3.

191. *Id.*

192. *Id.*

193. *Id.* at 7.

194. *European Chips Act: Commission launches Pilot System to Monitor Semiconductor Supply Chain*, EUR. COMM'N (May 10, 2023), <https://digital-strategy.ec.europa.eu/en/news/european-chips-act-commission-launches-pilot-system-monitor-semiconductor-supply-chain> [<https://perma.cc/BT8B-RKEL>] (“The Semiconductor Alert System will be included under the third pillar of the European Chips Act.”).

195. *Id.*

for a meticulous risk assessment and a prompt response to potential crises through the European Semiconductor Expert Group (ESEG).<sup>196</sup>

The recommendation accompanying the EU Chips Act led to the establishment of the European Semiconductor Expert Group (ESEG), which serves as a coordinating platform within the semiconductor supply chain.<sup>197</sup> It aids the EU Commission in executing existing and forthcoming regulatory frameworks effectively.<sup>198</sup> The efficacy of the alert system hinges on a precise appraisal of risks, heightened transparency within the supply chain, and enhanced resilience against disruptions.<sup>199</sup> This necessitates punctual access to information provided directly by companies through secure EU survey mechanisms, with exclusive accessibility limited to the European Commission.<sup>200</sup>

The Commission will scrupulously uphold the confidentiality of information obtained through this system.<sup>201</sup> Furthermore, measures will be instituted to respond appropriately to received information and, as necessary, engage with relevant stakeholders.<sup>202</sup> Following the full integration of this proposal into the EU Chips Act, the European Semiconductor Board will supplant the ESEG, which will be comprised of representatives from Member States and presided over by the European Commission.<sup>203</sup>

Following the track of the EU, the U.S. Department of Commerce introduced an updated Semiconductor Alert Mechanism in October 2023, overseen by the International Trade Administration (ITA), in line with President Biden's commitment to fortify resilient cross-border semiconductor supply chains.<sup>204</sup> This mechanism acts as a public-private platform for industry stakeholders to report disruptions, enabling Commerce to pinpoint bottlenecks in semiconductor supply chains.<sup>205</sup> This is anticipated to facilitate coordinated resource allocation to diminish chokepoint risks.<sup>206</sup> Companies and stakeholders are encouraged to share information on any microelectronics and semiconductor manufacturing disruptions, aiding in global supply chain resilience.<sup>207</sup>

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196. *EU Establishes Semiconductor Supply Chain 'Alert System'*, ASTUTE (May 18, 2023), <https://www.astutegroup.com/resources/eu-establishes-semiconductor-supply-chain-alert-system/> [<https://perma.cc/45E5-BBT9>].

197. *Id.*

198. *Id.*

199. *Id.*

200. *Id.*

201. Regulation 2023/1781 of the European Parliament and of the Council of Sept. 13, 2023, Establishing a Framework of Measures for Strengthening Europe's Semiconductor Ecosystem and Amending Regulation (EU) 2021/694 (Chips Act) (Text with EEA relevance), 2023 O.J. (L 229) 1, 40.

202. *Id.*

203. Commission Recommendation 2022/210 of Feb. 8, 2022, On a Common Union Toolbox to Address Semiconductor Shortages and an EU Mechanism for Monitoring the Semiconductor Ecosystem, 2022 O.J. (L 35) 17.

204. *Commerce Updates Semiconductor Alert Mechanism*, U.S. DEP'T OF COM. (Oct. 2, 2023), <https://www.commerce.gov/news/press-releases/2023/10/commerce-updates-semiconductor-alert-mechanism> [<https://perma.cc/2GTJ-CD4W>].

205. *Id.*

206. *Id.*

207. *Id.*

The semiconductor supply chain alert system is an emerging initiative designed to identify and address disruptions within the global semiconductor supply chain.<sup>208</sup> Although still in its early stages, it shows promise as a valuable tool for both the public and private sectors.<sup>209</sup> One of its key strengths lies in its collaborative nature, garnering support and endorsement from government authorities and the semiconductor industry.<sup>210</sup> This breadth of perspective and reach enhances its effectiveness in facilitating communication and coordination among diverse stakeholders within the supply chain.<sup>211</sup> Nonetheless, the alert system faces several potential challenges. The semiconductor supply chain's complexity and global dispersion pose significant hurdles in comprehensively tracking latent risk factors leading to disruptions.<sup>212</sup> Additionally, its early developmental stage necessitates rigorous evaluation and fine-tuning to identify and mitigate disruptions effectively.<sup>213</sup>

The alert system represents a promising venture with the potential to fortify the resilience of the global semiconductor supply chain.<sup>214</sup> It is crucial to approach it pragmatically, recognizing potential challenges and advocating for measures to enhance proficiency. These measures involve broadening the system's purview to encompass a comprehensive spectrum of stakeholders, refining algorithmic frameworks for enhanced disruption forecasting, and bolstering communication and coordination protocols among stakeholders.<sup>215</sup>

208. Ragonnaud, *supra* note 159, at 8–9.

209. See U.S. DEP'T OF COM, *supra* note 204 (discussing the advantages of the system for both businesses and consumers); See Alexandra Kelley, *Commerce and the International Trade Administration Encouraged Public and Private Organizations to Submit Reports on Disruptions in the Microelectronics' Supply Chain*, NEXTGOV/FCW (Oct. 3, 2023), <https://www.nextgov.com/modernization/2023/10/commerce-updates-semiconductor-supply-chain-alert-system/390892/> [<https://perma.cc/B98C-HQBQ>] (“The alert applies to both public and private sector entities, and focuses on disruptions in the global microelectronics and semiconductor supply chains. . . . Strengthening the U.S.’s semiconductor industry and supply chain flow is a central effort under the Biden administration.”).

210. See Federal Newswire Report, *Updates to the Semiconductor Alert System from the US Department of Commerce*, FED. NEWSWIRE (Oct. 11, 2023), <https://thefederalnewswire.com/stories/650268876-updates-to-the-semiconductor-alert-system-from-the-us-department-of-commerce> [[perma.cc/RW7Y-GBAZ](https://perma.cc/RW7Y-GBAZ)] (“The alert system is a public-private information-gathering technique that facilitates the expedited problem-solving process through collaboration with trading partners and the private sector.”).

211. *Id.* (conveying the reach and effectiveness of the system).

212. Wei Xiong et al., *Semiconductor Supply Chain Resilience and Disruption: Insights, Mitigation, and Future Directions*, INT’L JOURNAL OF PROD. RSCH. (Aug. 13, 2024); See e.g., Antonio Varas et al., *Strengthening the Global Semiconductor Supply Chain in an Uncertain Era*, BCG (Apr. 1, 2021), <https://www.bcg.com/publications/2021/strengthening-the-global-semiconductor-supply-chain> [<https://perma.cc/AT2F-BUK7>] (“[G]eographic specialization . . . creates vulnerabilities that each region needs to assess in a manner specific to its own economic and security considerations. There are more than 50 points across the supply chain where one region holds over 65% of the global market share . . .”).

213. See U.S. DEP'T OF COM., *supra* note 204 (noting that the US government set up an early system); See e.g. Vishal Gaur et al., *Research: Why It's So Hard to Map Global Supply Chains*, HARV. BUS. REV. (Oct. 31, 2022), <https://hbr.org/2022/10/research-why-its-so-hard-to-map-global-supply-chains> [[perma.cc/5YGP-4ZHL](https://perma.cc/5YGP-4ZHL)] (“Gaining supply chain visibility in such a complex network is an enormously difficult undertaking. . . . [T]he dynamic structure of the supply network means that firms have to keep updating their knowledge of supply chains and reassessing their risks continuously.”).

214. See U.S. DEP'T OF COM., *supra* note 204 (discussing advantages of the system); See Federal Newswire Report, *supra* note 210 (“This program is an important step toward assuring the long-term viability of semiconductor supply chains . . .”).

215. See, e.g., U.S. DEP'T OF COM., *supra* note 204 (“Commerce is calling on companies, manufacturers, and other interested parties to submit information regarding any new, ongoing, or potential disruptions to microelectronics and semiconductor manufacturing facilities and their related supply chains around the world.”).

Regular simulations, emulating real-world exigencies, should be employed to evaluate and strengthen the system's operational efficacy. Through diligent implementation of these strategies, the semiconductor supply chain alert system may be refined to a state of heightened effectiveness, advancing its capacity to shield the global semiconductor supply chain from prospective disruptions.<sup>216</sup>

#### D. Comparing Chips Acts in Europe and the U.S.

The CHIPS Act, along with the EU Chips Act, represent concerted legislative endeavors aimed at augmenting domestic semiconductor production while mitigating reliance on foreign suppliers.<sup>217</sup> Nonetheless, these two acts exhibit distinctive features.

With its broader ambit and larger budget, the CHIPS Act encompasses a much broader approach.<sup>218</sup> Conversely, the EU Chips Act focuses more on semiconductor-related initiatives.<sup>219</sup> The CHIPS Act encompasses provisions for scientific research and workforce development, extending its purview beyond the confines of semiconductor production.<sup>220</sup> Conversely, the EU Chips Act is more specifically tailored to semiconductors.<sup>221</sup> While both acts represent significant investments in domestic semiconductor production, nuanced distinctions arise.<sup>222</sup>

In terms of the provision of funding, the CHIPS Act allocates a total of \$280 billion for the facilitation of scientific research and development endeavors, of which an amount of \$52.7 billion is earmarked for semiconductor manufacturing and research and development, signifying a significant financial commitment to bolstering the sector.<sup>223</sup> In contrast, the EU Chips Act is poised to mobilize €43 billion (\$42.6 billion) from a combination of public and private sources.<sup>224</sup> It is imperative to underscore that the EU Chips Act will not directly

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216. See Federal Newswire Report, *supra* note 210 (“This program is an important step toward assuring the long-term viability of semiconductor supply chains, which is in accordance with the strategic goal of the administration to strengthen critical industries and to increase the economic resilience of the world as a whole.”).

217. See Stewart Wills, *A Tale of Two “Chips” Acts*, *Optica* at 26–27 (Nov. 11, 2022), [https://www.optica-opn.org/home/articles/volume\\_33/november\\_2022/departments/a\\_tale\\_of\\_two\\_chips\\_acts/](https://www.optica-opn.org/home/articles/volume_33/november_2022/departments/a_tale_of_two_chips_acts/) [<https://perma.cc/8BKW-SHHD>] (discussing the CHIPS act and EU Chips act).

218. See *id.* at 27–28 (stating how the act devoted \$52 billion to their project).

219. See *id.* at 28–29 (discussing the EU Chips Act and how they focus specifically on cutting-edge fabs and infrastructure).

220. See Shivakumar et al., *supra* note 28 (discussing the details of the CHIPS Act, including provisions for scientific research and workforce development).

221. See *id.* (“Themes include semiconductor research, pilot lines, standards, certification for energy efficiency and security of chips, skills, and networking of semiconductor research centers.”).

222. See *id.* (“While they have similar objectives, the U.S. and EU Chips Acts are distinguishable in a number of respects . . .”).

223. See PwC, *supra* note 85 (discussing the \$52.7 billion earmark for research and development); Alessandra Zimmermann, *R&D Funding Breakdown*, AAAS (Aug. 26, 2022), <https://www.aaas.org/sites/default/files/2023-01/CHIPS%20AAE.pdf> [<https://perma.cc/8H8C-34AQN2D2-DEYD>] (illustrating the overall funding for the act).

224. See Shivakumar et al., *supra* note 28 (“As noted above, the EU Chips Act involves at least €43 billion in identified public funding, with the expectation that this will spur a roughly equal amount of private investment.”).

provide all the funding.<sup>225</sup> Instead, it will leverage existing EU funding programs.<sup>226</sup>

The CHIPS Act incentivized companies such as Qualcomm and GlobalFoundries to set forth an ambitious goal of augmenting U.S. semiconductor manufacturing capacity by 50% within the ensuing five years.<sup>227</sup> In parallel, the EU Chips Act aspires to elevate the EU's global market share in semiconductors from 10% to 20% by 2030, signaling a substantial endeavor to strengthen the EU's position in the semiconductor market.<sup>228</sup> Viewed from this perspective, the CHIPS Act of the U.S. and the EU Chips Act exhibit a competitive dynamic, albeit potentially fostering productive outcomes in their domestic production bases.<sup>229</sup>

The European Commission has instigated a pilot endeavor termed “the Semiconductor Alert System” as part of the broader framework of the European Chips Act.<sup>230</sup> Initially, the CHIPS Act lacked such a provision.<sup>231</sup> Subsequently, the U.S. Department of Commerce introduced an enhanced semiconductor alert mechanism.<sup>232</sup>

It is imperative to underscore that while the CHIPS Act and the EU Chips Act constitute substantial strides toward mitigating reliance on foreign semiconductor suppliers, they do not present an effective panacea.<sup>233</sup> Establishing new semiconductor fabrication facilities necessitates time and substantial financial resources, implying that the full effects of these initiatives may not be immediately discernible.<sup>234</sup>

In the interim, the global semiconductor scarcity is anticipated to persist, potentially exerting adverse effects across a spectrum of industries,

225. *See id.* (stating how the funding will be provided by public and private sources).

226. *See id.* (“According to the European Union, the €43 billion in public funds will include some private money and only €3.3 billion from the European Union’s budget, making the composition of the Chips Act funding less distinct.”).

227. *See* THE WHITE HOUSE, *supra* note 15 (discussing how the passing of the act has spurred semiconductor companies into investing towards the goal of increasing U.S. semiconductor production).

228. *See* EUR. COMM’N, *supra* note 154 (conveying the goal of increasing production capacity to 20%); David Matthews, *EU Hails €80 Billion Intel Investment as First Success for Chips Act*, SCI. BUS. (Mar. 17, 2022), <https://sciencebusiness.net/news/eu-hails-eu80-billion-intel-investment-first-success-chips-act> [perma.cc/U8MR-K7A3] (“The EU’s Chips Act, launched last September, aims to more than double Europe’s share of the world market for semiconductors by 2030.”).

229. *See* EUR. COMM’N, *supra* note 154 (discussing the European Chips act); THE WHITE HOUSE, *supra* note 227 (discussing the U.S. CHIPS Act).

230. EUR. COMM’N, *supra* note 194; *See* Nick Flaherty, *EU Launches Semiconductor Supply Chain Alert System*, EENews (May 11, 2023), <https://www.eenewseurope.com/en/eu-launches-semiconductor-supply-chain-alert-system/> [perma.cc/B3KV-M5QP] (“The Semiconductor Alert System will be included under the third pillar of the European Chips Act, which aims to strengthen the preparedness and monitoring of the European semiconductor supply chain.”).

231. *See* Federal Newswire, *supra* note 210 (“The U.S. Department of Commerce has introduced an improved Semiconductor Alert Mechanism, which is supervised by the International Trade Administration, in keeping with President Biden’s unwavering commitment to strengthening strong international supply chains for semiconductors.”).

232. U.S. DEP’T OF COM., *supra* note 204.

233. *See* Shivakumar et al., *supra* note 28 (touching on the limitations of these acts).

234. *See id.* (discussing the time and financial limits of these acts).

encompassing consumer electronics, automotive, and healthcare.<sup>235</sup> A collaborative effort between governments and businesses is essential to ameliorate the impact of the shortage while concurrently constructing a more robust and resilient semiconductor supply chain for the future.<sup>236</sup>

#### IV. THE IMPLICATIONS OF MULTIPLE PATTERNING AND PARTICLE ACCELERATOR TECHNOLOGY ON CHIP MANUFACTURING

The integration of cutting-edge technologies in chip manufacturing is critical to meet the escalating demands for faster, more powerful, and energy-efficient chips.<sup>237</sup> Traditionally dominated by lithography, the semiconductor manufacturing field is now exploring particle accelerator technology as a transformative innovation.<sup>238</sup> This article describes the existing lithographic technology in chip manufacturing and explores the potential of particle accelerators in revolutionizing chip production, offering insights into how this approach could reshape the foundations of chip manufacturing.

In chip manufacturing, a crucial step is creating tiny circuits and transistors on the silicon wafer.<sup>239</sup> This is achieved through a process called photolithography, which uses light to define patterns on the wafer.<sup>240</sup> However, as chip designers keep pushing for smaller and more powerful devices, there is a physical limit to how small these features can be created with a single exposure of light.<sup>241</sup> Multiple patterning tackles this challenge by breaking down the desired pattern into multiple steps.<sup>242</sup> It essentially uses a series of lithography exposures, depositions, and etching processes to achieve a final pattern with features much smaller than the resolution of the light source itself.<sup>243</sup> This allows

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235. See generally Shivakumar et al., *supra* note 28 (“These parallel initiatives have been prompted by an awareness in both regions of threats to economic and strategic security arising out of their dependency on foreign-made chips.”).

236. See U.S. DEP’T OF COM., *supra* note 204 (exemplifying the collaboration between government and businesses).

237. See *2024 Vision: Semiconductor & Electronics Industry’s Comprehensive Brief*, ALLIED MKT. RSCH., <https://www.alliedmarketresearch.com/resource-center/trends-and-outlook/semiconductor-and-electronics/2024-vision-of-semiconductor-and-electronics-industry> [<https://perma.cc/6J2P-PH7K>] (last visited Sept. 15, 2024) (exemplifying current and future demands for semiconductor technology).

238. See *CLASSE Collaborates With Firm to Advance Semiconductor Manufacturing*, CLASSE (July 1, 2024), <https://www.classe.cornell.edu/news-events/news/classe-collaborates-firm-advance-semiconductor-manufacturing> [<https://perma.cc/78LL-V3UD>] (mentioning the use of particle accelerator technology in chip manufacturing); See, e.g., Norio Nakamura, et al. *Challenges Towards Industrialization of the ERL-FEL Light Source for EUV Lithography*, THPMP013 PROCEEDINGS OF THE 10TH INT. PARTICLE ACCELERATOR CONF. 3478–81 (2019) (“Energy-recovery linac based free-electron lasers (ERL- FELs) are possible candidates of a high-power EUV light source for lithography.”).

239. See Lucy Rodgers et al., *Inside the Miracle of Modern Chip Manufacturing*, FIN. TIMES (Feb. 27, 2024), <https://ig.ft.com/microchips/> [<https://perma.cc/ADH8-9U3Y>] (explaining the chip manufacturing process).

240. See *id.* (describing how photolithography is used in the chip-making process).

241. See Tim Bradshaw & Anna Gross, *The Big Question of How Small Chips Can Get*, FIN. TIMES (May 31, 2023), <https://www.ft.com/content/fbf52ede-e1a9-4797-9e52-3f80a7d855d9> [<https://perma.cc/GNU7-UK7J>] (discussing the problems manufacturers have when aiming for smaller chips).

242. See Xiaolin Wang et al., *supra* note 2 (discussing multiple patterning as a lithography method).

243. See Guojin Chen et al., *supra* note 3, at 1 (describing the multiple patterning process).

chipmakers to continue miniaturizing transistors and cramming more processing power into ever-shrinking chips.<sup>244</sup>

Another emerging technological development, particle accelerators, renowned for their role in high-energy physics experiments, possess unparalleled precision in manipulating subatomic particles.<sup>245</sup> This precision is directly applicable in chip manufacturing, where the ability to etch and implant materials at the atomic level is crucial.<sup>246</sup> By harnessing this precision, semiconductor manufacturers can push the boundaries of chip design, creating more compact, energy-efficient, and high-performance integrated circuits.

At the core of particle accelerators lies the capacity to propel particles at velocities approaching the speed of light. This has the potential to drastically reduce processing times in chip manufacturing. While conventional methods involve complex and time-consuming processes like photolithography and chemical etching, particle accelerator technology introduces a paradigm shift by enabling rapid and precise material manipulation. Consequently, the production cycle for semiconductor chips could be significantly shortened, leading to increased output and reduced time-to-market.

Energy efficiency has become a paramount concern in contemporary chip manufacturing. As chips become more powerful, managing excess heat has emerged as a significant challenge.<sup>247</sup> Particle accelerator technology offers a solution by enabling the development of chips with reduced power consumption.<sup>248</sup> Manufacturers can optimize transistor structures and layouts by employing precise particle beams for material modification, thereby minimizing leakage currents and improving overall energy efficiency.<sup>249</sup>

Particle accelerator technology also shows promise in addressing longstanding manufacturing challenges.<sup>250</sup> For instance, the miniaturization of

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244. See *ibid.* (stating how multiple patterning lithography can be used to continue miniaturizing chips).

245. See Sophie Bushwick, *New Particle Accelerator Fits on a Silicon Chip*, SCI. AM. (Jan. 4, 2020), <https://www.scientificamerican.com/article/new-particle-accelerator-fits-on-a-silicon-chip1/> [<https://perma.cc/D7ES-KQ3S>] (“Such a high-energy electron beam, produced at facilities such as California’s SLAC National Accelerator Laboratory, enables a variety of experiments, including capturing extremely detailed images and probing the structures of molecules.”).

246. See *id.* (“The miniature accelerator can, however, scale up much more easily than its larger counterpart: because it is etched in a small silicon wafer, researchers can fit multiple accelerating paths into future designs without adding bulk.”).

247. See Brian Bailey, *Getting Rid of Heat in Chips*, SEMICONDUCTOR ENG’G (July 20, 2023), <https://semiengineering.com/getting-rid-of-heat-in-chips/> [<https://perma.cc/K5G2-WTA6>] (“Power consumed by semiconductors creates heat, which must be removed from the device, but how to do this efficiently is a growing challenge.”).

248. See Anton Shilov, *China Aims to Use Particle Accelerators to Build Chips and Evade EUV Sanctions*, TOM’S HARDWARE (Sept. 26, 2023), <https://www.tomshardware.com/news/china-aims-to-use-particle-accelerator-to-build-chips-and-evade-euv-sanctions> [<https://perma.cc/J4ZG-J8AY>] (explaining how SSMB captures energy emitted during particle acceleration and the advantages to this method).

249. See MICHAEL CURRENT, *INDUSTRIAL ACCELERATORS AND THEIR APPLICATIONS* 48 (World Scientific, Aug. 2012) (discussing the efficiency of ion implementation).

250. See EFT Trends, *infra* note 252 (“The use of particle accelerators could aid in producing more chips for AI usage. This would help make China a world leader in the semiconductor manufacturing industry.”); see Stanford University, *Researchers Build a Particle Accelerator that Fits on a Chip*, PHYS ORG (Jan. 2, 2020), <https://phys.org/news/2020-01-particle-chip.html> [<https://perma.cc/XEW8-EYKA>] (suggesting that accelerator-on-a-chip prototype could make advancements in chemistry, materials science, biological discovery, and cancer radiation therapies).

semiconductor components has reached physical limits, posing hurdles for traditional fabrication methods.<sup>251</sup> Particle accelerators offer an avenue to bypass these limitations by enabling novel approaches to material deposition, doping, and patterning.<sup>252</sup> This innovative approach could pave the way for developing next-generation semiconductor devices with unprecedented capabilities.<sup>253</sup>

As the semiconductor industry continues its relentless pursuit of innovation, particle accelerator technology emerges as a potent force with the potential to redefine chip manufacturing.<sup>254</sup> By leveraging precision, speed, energy efficiency, and the ability to overcome longstanding manufacturing challenges, particle accelerators represent a transformative leap forward in semiconductor production.<sup>255</sup> As research and development efforts in this field continue to advance, a new era in chip manufacturing may be propelled by the extraordinary capabilities of particle accelerator technology.<sup>256</sup>

#### A. *Analyzing the Prevailing Process of Chip Manufacturing*

The process of chip manufacturing, also known as semiconductor fabrication, is a meticulously orchestrated sequence of steps aimed at crafting integrated circuits, the bedrock of modern electronic devices.<sup>257</sup> This process

251. See McFadden, *infra* note 294, at 3 (“Moore’s law . . . has been declared dead by some.”); see also Shara Tibken, *CES 2019: Moore’s Law is dead, says Nvidia’s CEO*, CNET (Jan. 9, 2019), <https://www.cnet.com/tech/computing/moores-law-is-dead-nvidias-ceo-jensen-huang-says-at-ces-2019/> [<https://perma.cc/5HV3-VN32>] (“A key part of semiconductor manufacturing is shrinking the components called transistors. . . . But as the scale of chip components gets closer and closer to that of individual atoms, it’s gotten harder to keep up the pace of Moore’s Law.”); see also Barrio & Sánchez-Somolinos, *infra* note 267, at 27 (“[t]o proceed toward further miniaturization, alternative approaches need to reach industrial production.”).

252. See ETF Trends, *Particle Accelerators Could Make China Semiconductors Leader*, NASDAQ (Sep. 29, 2023, 09:15 AM), <https://www.nasdaq.com/articles/particle-accelerators-could-make-china-semiconductors-leader> [<https://perma.cc/FS8J-Y8NV>] (“The use of particle accelerators could aid in producing more chips for AI usage.”).

253. See *id.* (“Using particle accelerators to create a novel laser source, researchers are laying the foundation for the future of semiconductor fabrication.”) (citation omitted).

254. See *id.* (“The use of particle accelerators could aid in producing more chips for AI usage. This would help make China a world leader in the semiconductor manufacturing industry.”); see also *China’s Giant Chip Factory Using Particle Accelerator to Challenge US Sanctions*, ABACHY SEMICONDUCTOR MATERIALS AND EQUIP., <https://abachy.com/news/chinas-giant-chip-factory-using-particle-accelerator-challenge-us> [<https://perma.cc/8B5K-U9D3>] (last visited Sept. 17, 2024) (explaining that particle accelerator researchers “aim to revolutionize semiconductor fabrication”).

255. See, e.g., *How Particle Accelerators Work*, DEP’T ENERGY (June 18, 2014) <https://www.energy.gov/articles/how-particle-accelerators-work> [<https://perma.cc/ULH8-DGUC>] (“A particle accelerator is a machine that accelerates elementary particles, such as electrons or protons, to very high energies.”); see also *id.* (“Worldwide, hundreds of industrial processes use particle accelerators . . . . Ion-beam accelerators, which accelerate heavier particles, find extensive use in the semiconductor industry in chip manufacturing . . . .”); see also ETF Trends, *supra* note 252 (“The use of particle accelerators could aid in producing more chips for AI usage. This would help make China a world leader in the semiconductor manufacturing industry.”).

256. See EFT Trends, *supra* note 252 (“The use of particle accelerators could aid in producing more chips for AI usage. This would help make China a world leader in the semiconductor manufacturing industry.”) see also Stanford University, *supra* note 250 (“[R]esearchers want to accelerate electrons to 94 percent of the speed of light . . . to create a particle flow powerful enough for research or medical purposes.”).

257. Daniel Neumaier et al., *Integrating Graphene into Semiconductor Fabrication Lines*, 18 NATURE MATERIALS, 525–29 (2019) (describing the specific steps of making semiconductors in order to argue that integrating graphene would be beneficial to that process).

encapsulates numerous stages, each contingent on cutting-edge materials, precision equipment, and intricate methodologies.<sup>258</sup> The following is the process of chip manufacturing based on the dominant ASML-TSMC nexus, including various stages such as ingot formation, lithography, deposition, annealing, and packaging.<sup>259</sup>

### 1. *Crystal Growth and Ingot Formation*

At the genesis of chip manufacturing lies the cultivation of silicon crystals, often referred to as ingots.<sup>260</sup> This process, known as the Czochralski or the Float Zone method, involves the controlled solidification of molten silicon, yielding a cylindrical crystal structure of exceptional purity and crystalline uniformity.<sup>261</sup>

### 2. *Wafer Slicing*

The resultant silicon ingot undergoes precise slicing into ultra-thin wafers, each serving as a substrate for individual chips.<sup>262</sup> Advanced diamond saws, utilizing abrasive slurry, effectuate this process, ensuring wafers of uniform thickness.<sup>263</sup>

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258. See *How Microchips Are Made*, ASML, <https://www.asml.com/en/technology/all-about-microchips/how-microchips-are-made> [<https://perma.cc/4CZ4-RNWX>] (last visited Sept. 17, 2024) (“The microchip manufacturing process involves hundreds of steps . . . . Our latest-generation EUV . . . machines are used for the most critical layers. . .”).

259. See Alison Li & Jessica Timings, *6 Crucial Steps in Semiconductor Manufacturing*, ASML (Oct. 4, 2023), <https://www.asml.com/en/news/stories/2021/semiconductor-manufacturing-process-steps> [<https://perma.cc/E5YL-T8X9>] (“Let’s discuss six critical semiconductor manufacturing steps: deposition, photoresist, lithography, etch, ionization and packaging.”); see also SZE & LEE, *infra* note 260, at 492 (“Annealing is a heat treatment that alters the microstructure of a material, causing changes in properties.”).

260. See, e.g., SIMON M. SZE & MING-KWEI LEE, *Semiconductor Devices: Physics and Technology* 357 (3rd ed. 2012) (“The single-crystal ingots. . . .”) see also *ibid.* (“[T]he two most important semiconductors for discrete devices and integrated circuits are silicon and gallium arsenide. . . . [W]e describe the common techniques for growing single crystals of these two semiconductors.”); see also Bates & Moll, *infra* note 261, at 113 (“Almost all detectors currently used in HEP use silicon grown by the Float Zone (FZ) technique.”).

261. See Alison G. Bates & Michael Moll, *A Comparison Between Irradiated Magnetic Czochralski and Float Zone Silicon Detectors Using the Transient Current Technique*, 555 *NUCLEAR INSTRUMENTS & METHODS PHYSICS RSCH.: SECTION A* 113, 113 (2005) (“The FZ growth method yields high purity and high-resistivity silicon . . . .”); see also SZE & LEE, *supra* note 260, at 357–58 (describes in detail the “Czochralski technique”); see also *idid.* at 363 (“The float-zone process can be used to grow silicon that has lower contamination than that normally obtained from the Czochralski technique.”).

262. See GARY S. MAY & COSTAS J. SPANOS, *FUNDAMENTALS OF SEMICONDUCTOR MANUFACTURING AND PROCESS CONTROL*, 9 (2006) (figure 1.4 shows the use of a silicon wafer); see also SZE & LEE, *supra* note 260, at 371 (“The ingot is now ready to be sliced by diamond saw into wafers.”).

263. See Jintao Zheng et al., *Action Mechanism of Liquid Bridge Between Electroplated Diamond Wires for Ultrathin Wafer Slicing.*, 231 *SOLAR ENERGY* 343, 343 (2022) (“[D]iamond wire sawing . . . can enhance yield by reducing the wafer slicing thickness . . . .”); see also SZE & LEE, *supra* note 260, at 421 (CMP allows the creation of a “flat surface across the whole wafer” by using the “[a]brasive particles in the slurry”).

### 3. *Cleaning and Polishing*

Following slicing, the wafers undergo rigorous cleaning procedures to eliminate impurities.<sup>264</sup> This entails immersion in chemical solutions and the application of high-purity water, ensuring a pristine substrate for subsequent processing steps.<sup>265</sup> Polishing then refines the wafer surface to an atomic-level smoothness.<sup>266</sup>

### 4. *Photolithography*

Photolithography stands as a linchpin in semiconductor fabrication.<sup>267</sup> It involves the projection of intricate circuit patterns onto the wafer's surface via photomasks, defining the circuitry's layout.<sup>268</sup> This step governs critical dimensions and dictates the chip's functionality.<sup>269</sup>

### 5. *Etching*

Etching, a pivotal step subsequent to photolithography, involves the selective removal of material from the wafer's surface.<sup>270</sup> Chemical or plasma etching methods are employed to delineate the desired circuitry patterns, allowing for a precise definition of features.<sup>271</sup>

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264. See SZE & LEE, *supra* note 260, at 371 (“The final step of wafer shaping is polishing. Its purpose is to provide a smooth, specular surface where device features can be defined by lithographic processes. . . .”); see also MAY & SPANOS, *supra* note 262, at 47 (“Semiconductor wafers are chemically cleaned to remove contamination that results from handling and storing.”).

265. CHUE SAN YOO, SEMICONDUCTOR MFG. TECH. 91 (W. K. Chen ed., 2008) (“Cleaning is the most frequently repeated step in a semiconductor manufacturing line.”).

266. See, e.g., SZE & LEE, *supra* note 260, at 371 (“The final step of wafer shaping is polishing. Its purpose is to provide a smooth, specular surface where device features can be defined by lithographic processes. . . .”).

267. See Jesús del Barrio & Carlos Sánchez-Somolinos, *Light to Shape the Future: From Photolithography to 4D Printing*, 7 ADVANCED OPTICAL MATERIALS 1, 9 (2019) (“Mask photolithography has been crucial in the development of the microelectronics industry.”).

268. See *ibid.* (“In the most traditional photolithographic process, the image of a mask . . . is transferred to the photosensitive material to create the desired polymeric structure on the target substrate. . . .”); see also *ibid.* (“The image of the mask with the structure of an integrated circuit . . . is transferred to a thin photoresist layer applied on top of a silicon wafer . . . leading to a polymeric surface relief structure.”).

269. STANLEY WOLF & RICHARD N. TAUBER, *Silicon Processing for the VLSI Era: Volume 1—Process Technology* 488 (2nd ed. 2000) (“[m]icrocircuit fabrication requires precisely controlled quantities of impurities to be introduced into tiny regions of the silicon substrate . . . these regions must be interconnected to create components and VLSI circuits.”).

270. See Thorsten Lill & Olivier Joubert, *The Cutting Edge of Plasma Etching*, 319 SCIENCE MAG 1050, 1050 (2008) (“To create structures in a chip, a pattern is formed in a photoresist by lithography and then transferred into the device materials by plasma etching.”); see also SZE & LEE, *supra* note 260, at 428 (“Lithography is the process of transferring patterns. . . . The pattern transfer is accomplished by an etching process that selectively removes unmasked portions of a layer.”) (footnote omitted).

271. See Lill & Joubert, *supra* note 270 (“[P]lasma etching . . . us[es] lateral erosion of the lithographic photoresist to improve resolution. . . .”); see also SZE & LEE, *supra* note 260, at 447 (describing chemical etching and its “three essential steps”).

## 6. *Deposition*

Chip manufacturing requires various materials to be deposited onto the wafer's surface to form distinct layers.<sup>272</sup> Techniques like chemical vapor deposition (CVD) and physical vapor deposition (PVD) are employed to create conductive, insulating, and semiconducting layers as the chip's design dictates.<sup>273</sup>

## 7. *Doping*

Doping entails the introduction of impurities into specific regions of the wafer to alter its electrical properties.<sup>274</sup> This process creates conductive paths and establishes the transistor functionality crucial to chip operation.<sup>275</sup>

## 8. *Annealing*

Annealing subjects the wafer to controlled heating, allowing dopants to diffuse and stabilize within the crystal lattice.<sup>276</sup> This step optimizes electrical characteristics, ensuring consistent performance across the chip.<sup>277</sup>

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272. See Kangning Ren et al., *Materials for Microfluidic Chip Fabrication*, 46 ACCTS. CHEM. RSCH. 2396, 2396 (2013) (“In this Account, we address the evolution of materials used for fabricating microfluidic chips, and discuss the application-oriented pros and cons of different materials.”).

273. See Yuchao Bai et al., *Investigation on the Microstructure and Machinability of ASTM A131 Steel Manufactured by Directed Energy Deposition*, 276 J. MATERIALS PROCESSING TECH. 1, 11 (2020) (“This paper presents a method to achieve high-quality metal parts by additive and subtractive manufacturing technologies.”); see also SZE & LEE, *supra* note 260, at 400 (“Deposited dielectric films are used mainly for insulation . . . of discrete devices and integrated circuits. Considerations in selecting a deposition process are . . . electrical and mechanical properties . . .”); see also *ibid.* (“Chemical vapor deposition (CVD) is the most useful method for the deposition of a wide variety of thin films in semiconductor device fabrication.”); see also *id.* at 414 (“The primary semiconductor applications of physical-vapor deposition (PVD) technology are the deposition of metal and compounds . . . for lines, pads, vias, contacts, and related connections that are used to connection with the junctions and devices on the Si wafer surface.”).

274. See, e.g., Rodolfo Peña-Rodríguez et al., *Doping of a Zn-MOF with Eu<sup>3+</sup> and Tb<sup>3+</sup> for Application in the Manufacture of a WLED*, 9 J. MATERIALS CHEMISTRY C 15891, 15898 (2021) (“In summary, we used formic acid and zinc nitrate to synthesize a porous and blue light-emitting MOF, which was doped with Eu<sup>3+</sup> and Tb<sup>3+</sup> . . .”); see also SZE & LEE, *supra* note 260, at 466 (“Impurity doping is the introduction of controlled amounts of impurity dopants into semiconductor materials. The practical use of impurity doping is primarily to change the electrical properties of the semiconductors.”).

275. See SZE & LEE, *supra* note 260, at 208 (“The heavily doped substrate provides a highly conductive path to collect the current.”); see also *id.* at 466 (“Impurity doping is the introduction of controlled amounts of impurity dopants into semiconductor materials. The practical use of impurity doping is primarily to change the electrical properties of the semiconductors.”).

276. See *id.* at 491–92 (“To activate the implanted ions and restore mobility and other material parameters, we must anneal the semiconductor . . . . Annealing is a heat treatment that alters the microstructure of a material, causing changes in properties.”).

277. *Id.*; see also V. Venugopal & T. T. Narendran, *Cell Formation in Manufacturing Systems Through Simulated Annealing: an Experimental Evaluation*, 63 EUR. J. OPERATIONAL RSCH. 409, 409 (1992) (“Simulated annealing is a general random search method for finding near-global optimal solutions for optimization problems . . .”).

### 9. *Testing and Packaging*

Post-fabrication, chips undergo exhaustive testing to detect and rectify defects.<sup>278</sup> Subsequently, they are encapsulated in protective packages, shielding them from environmental factors and facilitating integration into electronic systems.<sup>279</sup>

### 10. *Inspection and Quality Assurance*

The manufactured chips undergo a rigorous final inspection to ensure adherence to specifications and quality benchmarks.<sup>280</sup> This phase involves comprehensive electrical testing, visual inspection, and performance validation.<sup>281</sup>

The lithographic chip manufacturing process is a sophisticated amalgamation of material science, precision engineering, and intricate process technologies.<sup>282</sup> The resultant integrated circuits power the breadth of modern electronic devices, underpinning the digital infrastructure that permeates contemporary society.<sup>283</sup>

#### B. *The Dominance of the ASML-TSMC Nexus*

The chip manufacturing industry is dominated by two non-American companies, ASML (Advanced Semiconductor Materials Lithography) and Taiwan Semiconductor Manufacturing Company (TSMC).<sup>284</sup> This ASML-

278. See SZE & LEE, *supra* note 260, at 506 (“Prior to chip separation, each chip is electrically tested. Defective chips are usually marked. . . . Good chips are selected and packaged . . .”).

279. See SHENG LIU & XIAOBING LUO, LED PACKAGING FOR LIGHTING APPLICATIONS: DESIGN, MANUFACTURING AND TESTING 36–37 (2011) (describing “wafer level packaging” in detail); see also *id.* at 52 (describing the value of packaging the chip); see also SZE & LEE, *supra* note 260, at 506 (“Good chips are selected and packaged to provide an appropriate thermal, electrical, and interconnection environment for electronic applications.”) (footnote omitted).

280. See, e.g., SZE & LEE, *supra* note 260, at 506 (“Prior to chip separation, each chip is electrically tested. Defective chips are usually marked. . . . Good chips are selected and packaged . . .”); see also Hannah Casper et al., *The Impact of the Computer Chip Supply Shortage*, PROC. INT’L CONF. ON INDUS. ENG’G AND OPERATIONS MGMT. BANGALORE, INDIA, 236, 237 (2021) (“Production of semiconductors occurs in three major steps: design, fabrication, and ATP. ATP stands for assembly, testing, and packaging.”) (citation omitted).

281. See SZE & LEE, *supra* note 260, at 506 (“Prior to chip separation, each chip is electrically tested. Defective chips are usually marked. . . . Good chips are selected and packaged . . .”); see also *Measuring Accuracy*, ASML, <https://www.asml.com/en/technology/lithography-principles/measuring-accuracy> [<https://perma.cc/5NXJ-UQYY>] (last visited Sep. 9, 2024) (ASML uses “e-beam metrology” to inspect chips for defects).

282. See Casper et al, *supra* note 280, at 237 (describing the numerous steps, materials, components, and methods which go into chip production).

283. See *id.* at 236 (“The use of computer chips has become widespread across different industries, with each industry attempting to secure its own supply.”); see also *id.* at 242 (“[a]s chip requirements rise for vehicles, the consumer electronics industry is also increasingly reliant on chips to meet the demand for personal electronics such as phones and laptops.”).

284. See Casper et al, *supra* note 280, at 237 (“Taiwan Semiconductor Manufacturing Company (TSMC) created the first dedicated semiconductor foundry. . . . TSMC is contracted by large companies like Apple to produce the chips companies design.”); see also ASML, *infra* note 291 (ASML has over forty-thousand employees and over sixty locations); see also *History: Over 40 Years of Ingenuity and Perseverance*, ASML <https://www.asml.com/en/company/about-asml/history> [<https://perma.cc/LZB9-9W7R>] (last visited Sept. 14,

TSMC nexus in semiconductor fabrication embodies a formidable convergence of two eminent entities within the industry’s vanguard.<sup>285</sup> ASML, distinguished for its preeminence in photolithographic machinery, plays a pivotal role in the realization of integrated circuits (ICs).<sup>286</sup> TSMC, conversely, stands as a preeminent foundry specializing in semiconductor fabrication for a diverse clientele.<sup>287</sup>

The amalgamation of ASML’s forefront lithographic technology with TSMC’s manufacturing proficiency engenders an exceptionally streamlined and technologically sophisticated conduit for IC production.<sup>288</sup> This symbiosis culminates in the realization of semiconductor devices at infinitesimal process nodes, culminating in heightened performance, power efficiency, and an expanded spectrum of applications across multifarious sectors.<sup>289</sup> This

2024) (since the early 2000s ASML has continually acquired various tech companies to improve semiconductor manufacturing); *see also* *Largest Semiconductor Companies by Market Cap*, COMPANIES MARKETCAP, <https://companiesmarketcap.com/semiconductors/largest-semiconductor-companies-by-market-cap/> [<https://perma.cc/9Y62-XXAB>] (last visited Sept. 17, 2024) (displaying the first non-USA companies as TSMC and ASML).

285. *See* ASML (*Inside a Semiconductor Industry Leader*), *infra* note 286 (“We provide chipmakers with everything they need—hardware, software and services—to mass produce patterns on silicon through lithography.”); *see also id.* (“ASML and imec open joint High NA EUV Lithography Lab offering an early development platform to the leading-edge semiconductor ecosystem.”); *see also* TSMC, *infra* note 287 (“In 2023, TSMC served 528 customers and manufactured 11,895 products for various applications covering a variety of end markets including high performance computing, smartphones, the Internet of Things (IoT), automotive, and digital consumer electronics.”).

286. *See* *Inside a Semiconductor Industry Leader*, ASML, <https://www.asml.com/en/company> [<https://perma.cc/R76Q-M6LS>] (last visited Sept. 16, 2024) (“We provide chipmakers with everything they need—hardware, software and services—to mass produce patterns on silicon through lithography.”); *see also* *The Basics of Microchips*, ASML, <https://www.asml.com/en/technology/all-about-microchips/microchip-basics> [<https://perma.cc/TYR2-8J3G>] (last visited Sept. 16, 2024) (“A microchip (also called a chip, a computer chip, an integrated circuit or IC) is a set of electronic circuits on a small flat piece of silicon.”); *see also* *DUV Lithography Systems*, ASML, <https://www.asml.com/en/products/duv-lithography-systems> [<https://perma.cc/V6DT-K6MU>] (last visited Sept. 16, 2024) (“ASML’s deep ultraviolet (DUV) lithography systems dive deep into the UV spectrum to print the tiny features that form the basis of the microchip.”).

287. *See* *About TSMC*, TSMC, <https://www.tsmc.com/english/aboutTSMC> [<https://perma.cc/V8PQ-SRVA>] (last visited, Sept. 17, 2024) (“In 2023, TSMC served 528 customers and manufactured 11,895 products for various applications covering a variety of end markets including high performance computing, smartphones, the Internet of Things (IoT), automotive, and digital consumer electronics.”); *see also* *Unleash Innovation*, TSMC, <https://www.tsmc.com/english/dedicatedFoundry/technology> [<https://perma.cc/9U6Y-NG3W>] (last visited Sept. 17, 2024) (“TSMC has the broadest range of technologies and services in the Dedicated IC Foundry segment of the semiconductor manufacturing industry.”).

288. *TSMC and ASML Reach Agreement to Develop Next Generation Lithography Technologies as an Extension of Long-Term Partnership*, TSMC (Aug. 5, 2012), <https://pr.tsmc.com/english/news/1734> [<https://perma.cc/V7AV-LDAY>]; *see* ASML, *supra* note 286 (“We provide chipmakers with everything they need—hardware, software and services—to mass produce patterns on silicon through lithography.”); *see also id.* (“ASML and imec open joint High NA EUV Lithography Lab offering an early development platform to the leading-edge semiconductor ecosystem.”); *see also* TSMC, *supra* note 287 (“In 2023, TSMC served 528 customers and manufactured 11,895 products for various applications covering a variety of end markets including high performance computing, smartphones, the Internet of Things (IoT), automotive, and digital consumer electronics.”).

289. Venkatesh Jartakar, *TSMC and ASML Navigate Headwinds Amid Semiconductor Industry Growth*, INVESTING (Oct. 24, 2023), <https://www.investing.com/news/stock-market-news/tsmc-and-asml-navigate-headwinds-amid-semiconductor-industry-growth-93CH-3206930> [<https://perma.cc/5BKF-8CXT>] (“The symbiotic relationship between the two companies has been instrumental in driving efficiency and miniaturization in chip production.”); *see also* *EUV Lithography Systems*, ASML, <https://www.asml.com/en/products/euv-lithography-systems> [<https://perma.cc/4ZX6-THUW>] (last visited Sep.

formidable collaboration serves to cement ASML and TSMC's stature as vanguards in the semiconductor domain, catalyzing innovation and propelling technological progress.<sup>290</sup>

### 1. ASML (*Advanced Semiconductor Materials Lithography*)

Established in 1984 as a joint venture between Philips and ASM International, ASML is a leading manufacturer of chip-making equipment, with a particular focus on the pivotal role of lithography machines in chip production.<sup>291</sup> Headquartered in Veldhoven, the Netherlands, it boasts over 39,000 employees globally, with more than 16,800 based at its headquarters.<sup>292</sup> Notable clients, including Intel, employ ASML's machines to manufacture microchips for diverse electronic devices.<sup>293</sup>

ASML's dominance in lithography technology stems from extensive research and development efforts and an innovative ethos.<sup>294</sup> The company has invested substantially in cultivating engineering expertise, establishing advanced research facilities, and harnessing cutting-edge technologies to refine and advance lithographic processes.<sup>295</sup> A crucial factor lies in ASML's unwavering dedication solely to lithographic technology.<sup>296</sup> This focused commitment has enabled ASML to elevate the precision and sophistication of its lithography machinery to an extraordinary degree.<sup>297</sup>

The technical complexity inherent in DUV and EUV lithography necessitates a substantial reservoir of intellectual property, spanning optical systems to precision engineering and materials science.<sup>298</sup> ASML's extensive

16, 2024) ("EUV lithography does big things on a tiny scale. The technology, which is unique to ASML, prints microchips using light with a wavelength of just 13.5 nm. . . . EUV is driving Moore's Law forward and supporting novel transistor designs and chip architectures.").

290. For the collaboration between ASML and TSMC see Jane Lee & Stephen Nellis, *TSMC Says It Will Have Advanced ASML Chipmaking Tool in 2024*, REUTERS (June 16, 2022, 06:07 PM), <https://www.reuters.com/technology/tsmc-says-it-will-have-advanced-asml-chipmaking-tool-2024-2022-06-16/> [https://perma.cc/LEK9-UMGL] ("[TSMC] executives said on Thursday the world's biggest chipmaker will have the next version of ASML Holding NV's most advanced chipmaking tool in 2024."); see also Naomi Buchanan, *TSMC Likely to Receive ASML Chipmaking Machine this Year, Stocks Jump*, INVESTOPEDIA (June 5, 2024, 01:23 PM), <https://www.investopedia.com/tsmc-likely-to-receive-asml-chipmaking-machine-this-year-stocks-jump-8658578> [https://perma.cc/CWJ6-EQBX] ("[A]nalysts reported that the Dutch firm [ASML] is optimistic that TSMC will receive its advanced chipmaking machine this year.").

291. This is based on the information provided in the ASML's website, *About ASML*, ASML, <https://www.asml.com/en/company/about-asml> [https://perma.cc/Y9BX-MDSP] (last visited Sept. 16, 2024).

292. *Id.*

293. *Id.*

294. Christopher McFadden, *A New 'Extreme Ultraviolet' Microchip Machine Could Revive Moore's Law*, INTERESTING ENG'G. (Sept. 02, 2021, 8:48 PM), <https://interestingengineering.com/innovation/new-extreme-ultraviolet-microchip-machine-could-revive-moores-law> [https://perma.cc/C34T-T3HX].

295. *ASML Opens New State-of-the-Art R&D Facility in Silicon Valley*, ASML, <https://www.asml.com/en/news/press-releases/2021/asml-expands-presence-in-silicon-valley-with-new-campus> [https://perma.cc/NZA2-8FL7] (last visited Sept. 16, 2024).

296. *Id.*; Jessica Timings, *TWINSCAN: 20 Years of Lithography Innovation*, ASML (Aug. 18, 2021), <https://www.asml.com/en/news/stories/2021/twincan-20-years-innovation> [https://perma.cc/X9XZ-4VWF].

297. Ekta Sharma et al., *Evolution in Lithography Techniques: Microlithography to Nanolithography*, 12 NANOMATERIALS 1, 10 (2022).

298. See generally Sophie Bushwick, *supra* note 245 (describing technological impact particle accelerators can have on microchip development).

portfolio of patents and proprietary technologies significantly contributes to its competitive advantage, forming a formidable barrier to entry.<sup>299</sup> ASML's steadfast commitment to the financial support of research, development, and manufacturing facilities has bolstered its position as a technological vanguard.<sup>300</sup>

ASML's preeminence in producing DUV and EUV lithography machines arises from a confluence of factors, including focused specialization, strategic collaborations, extensive intellectual property, substantial financial investments, and an unwavering commitment to advancing lithography technology.<sup>301</sup> This integrative approach has solidified ASML's stature as a global frontrunner in lithographic solutions, presenting a considerable challenge for American enterprises seeking to replicate their success in this highly specialized field.<sup>302</sup>

Despite ASML's dominance, in November 2023, Canon, a prominent Japanese company known for printers and cameras, introduced the FPA-1200NZ2C, a cutting-edge nanoimprint lithography system.<sup>303</sup> This technology aims to revolutionize semiconductor manufacturing, challenging the dominance of ASML in ultraviolet lithography.<sup>304</sup> FPA-1200NZ2C promises semiconductor production with a 5-nanometer process, reaching an impressive 2 nanometers, showcasing the reality that ASML's competitors are committed to advancing technological frontiers in the semiconductor industry.<sup>305</sup> Of course, this includes the challenges of the development of particle accelerator technology in China.<sup>306</sup>

Canon's FPA-1200NZ2C asserts the capability to engage in semiconductor manufacturing processes characterized by a 5-nanometer precision, with the capacity to achieve an exceptional scale as diminutive as 2 nanometers.<sup>307</sup> This substantiates the assertion that competitors to ASML, notably Canon, evince a resolute dedication to the progressive evolution of technological boundaries within the semiconductor industry.<sup>308</sup> This commitment extends to navigating

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299. See generally Radu Donose et al., *Additive manufacturing in ASML lithography machines: benefits and quality assurance*, EUSPN (Sept. 2023) (discussing productivity implications with new technology).

300. *Id.*

301. Mario Gabriele, *ASML: A Monopoly on Magic*, THE GENERALIST (July 30, 2023), <https://www.generalist.com/briefing/asml> [<https://perma.cc/74LK-KS5S>] (describing the history of ASML and their focus on location, connections, and supply chain operations).

302. Kumar Priyadarshi, *How ASML's EUV Lithography Technology Made It Europe's Most Valuable Company*, TECHOVEDAS (Aug. 17, 2023), <https://techovedas.com/how-asmls-euv-lithography-technology-made-it-europes-most-valuable-company/> [<https://perma.cc/8WVF-L24E>] (describing US chip makers attempts at EUV lithography technology in the 1980s and 1990s).

303. Arjun Kharpal, *Canon, Known for Its Cameras, Launches ASML Challenge with Machine to Make the Most Advanced Chips*, CNBC (Oct. 13 2023, 7:08 AM), <https://www.cnbc.com/2023/10/13/canon-launches-asml-challenge-with-machine-to-make-most-advanced-chips.html> [<https://perma.cc/WHF4-FMFV>].

304. See *id.* (characterizing the FPA-1200NZ2C as a challenge to ASML).

305. See *id.* (discussing the capabilities of Canon's technology).

306. See *id.* (discussing limits to manufacturing in China).

307. *Id.*

308. *Id.* See also *Semiconductor Lithography Equipment*, CANON, [https://global.canon/en/technology/s\\_labo/light/003/09.html](https://global.canon/en/technology/s_labo/light/003/09.html) [<https://perma.cc/3EBM-Q4S3>] (last visited Sept. 17, 2024) (discussing Canon's developing technology).

challenges posed by concurrent advancements, such as those observed in particle accelerator technology emanating from China.<sup>309</sup>

## 2. TSMC (Taiwan Semiconductor Manufacturing Company)

TSMC's preeminence in high-end semiconductor fabrication arises from a synergy of key factors. Notably, TSMC leads the chip industry through its foundry business model, substantial research and development investments, advanced process technology, and extensive production capacity.<sup>310</sup>

Central to TSMC's dominance is its unwavering commitment to technological innovation and research.<sup>311</sup> This has established TSMC as a leader in chip manufacturing proficiency, particularly in the 3nm FinFET (N3) technology.<sup>312</sup> This advancement represents a significant leap from its predecessor, the 5nm generation.<sup>313</sup> TSMC's trajectory includes the refinement of 3nm processes, such as N3E and N3P, to enhance power efficiency, performance, and density metrics.<sup>314</sup> Additionally, specialized processes like N3X for high-performance computing and N3AE for automotive applications are underway.<sup>315</sup>

TSMC's strategic collaborations and substantial investments in the U.S. have solidified its pivotal role in the American semiconductor supply chain.<sup>316</sup> Unlike Intel, which primarily focuses on proprietary designs, TSMC's "pure-play" foundry model involves manufacturing chips for various companies, including those without in-house manufacturing capacities.<sup>317</sup> Moreover, TSMC's extensive production capacity and operational flexibility position it as a linchpin in the global chip production ecosystem.<sup>318</sup> This capacity and

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309. Leo Sun, *Could Canon Become the Next ASML?*, THE MOTLEY FOOL (Oct. 18, 2023, 9:00 AM), <https://www.fool.com/investing/2023/10/18/could-canon-become-the-next-asml/>; see generally S. V. Kutsaev, *Advanced Technologies for Applied Particle Accelerators and Examples of their Use*, 66 TECH. PHYSICS 161–95 (2021) (citing Chinese sources while discussing current technological developments).

310. TSMC, *supra* note 287.

311. *Id.*

312. See *3nm Technology*, TSMC, [https://www.tsmc.com/english/dedicatedFoundry/technology/logic/l\\_3nm](https://www.tsmc.com/english/dedicatedFoundry/technology/logic/l_3nm) [<https://perma.cc/MBM8-M83S>] (last visited Sept. 17, 2024) (“As a global semiconductor technology leader, TSMC provides the most advanced and comprehensive portfolio of dedicated foundry process technologies.”).

313. *Id.*

314. See Anton Shilov, *TSMC Details 3nm Evolution: N3E On Schedule, N3P and N3X To Deliver 5% Performance Gains*, ANANDTECH (Apr. 26, 2023, 5:15PM), <https://www.anandtech.com/show/18833/tsmc-details-3nm-evolution-n3e-on-schedule-n3p-n3x-deliver-five-percent-gains> [<https://perma.cc/9JXS-T4F9>] (detailing TSMC announcements concerning N3E, N3P, and N3X process nodes).

315. *Id.*

316. See *TSMC Arizona and U.S. Department of Commerce Announce up to US\$6.6 Billion in Proposed CHIPS Act Direct Funding, the Company Plans Third Leading-Edge Fab in Phoenix*, TSMC (Apr. 8, 2024), <https://pr.tsmc.com/english/news/3122> [<https://perma.cc/3TVC-HU3P>] (last visited Sept. 16, 2024) (discussing U.S. government's strategic investment in TSMC).

317. See *TSMC Founded – The First Pure-Play Foundry*, THE CHIP HIST. CTR., <https://www.chiphistory.org/527-tsmc-founded-the-first-pure-play-foundry> [<https://perma.cc/PR2F-EV35>] (last visited Sept. 17, 2024).

318. Kathrin Hille, *TSMC: How a Taiwanese Chipmaker Became a Linchpin of the Global Economy*, FIN. TIMES (Mar. 24, 2021), <https://www.ft.com/content/05206915-fd73-4a3a-92a5-6760ce965bd9> [<https://perma.cc/FD3F-XDCU>]; Chris Miller, *The Chips That Make Taiwan the Center of the World*, TIME (Oct.

sophisticated manufacturing facilities allow TSMC to accommodate a diverse array of chip designs and manufacturing requisites, giving it a competitive edge over its counterparts.<sup>319</sup>

TSMC's advancements in process technology, enabling the production of chips with smaller transistor dimensions and enhanced operational efficiency, further reinforce its competitive edge.<sup>320</sup> The support from both the Taiwanese and U.S. governments has played a crucial role in fostering TSMC's enduring footprint.<sup>321</sup> TSMC's steadfast commitment to innovation, demonstrated through perpetual research and development initiatives, underscores its competitive advantage.<sup>322</sup> Its capacity to meet the growing demand for advanced semiconductor technology in areas like artificial intelligence, 5G telecommunications, and high-performance computing has solidified its stature in the market.<sup>323</sup>

TSMC received favorable support from the U.S. government.<sup>324</sup> For instance, in October 2023, Taiwan's Minister of Economic Affairs, Mei-Hua Wang, confirmed TSMC's one-year exemption from the U.S. ban on exporting semiconductor chips to China, enabling its uninterrupted operations in the country.<sup>325</sup> The U.S. Department of Commerce's Bureau of Industry and Security (BIS) has suggested that TSMC apply for the "validated end-user" (VEU) program, streamlining export approvals.<sup>326</sup> It is suggested that as long as TSMC refrains from major technological upgrades in its Chinese facilities, it will maintain this privilege.<sup>327</sup> Wang emphasized TSMC's commitment to protecting trade secrets and compliance with regulations.<sup>328</sup> The company's cutting-edge manufacturing and research are based in Taiwan and supported by various governments, including the U.S. and Japan.<sup>329</sup>

TSMC's preeminence in high-end chip manufacturing is underpinned by technological leadership, strategic interdependencies, globalized supply chain

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5, 2022, 6:00 AM), <https://time.com/6219318/tsmc-taiwan-the-center-of-the-world/> [<https://perma.cc/6FWC-57UG>].

319. See *TSMC Arizona*, TSMC, <https://www.tsmc.com/static/abouttsmcaz/index.htm> [<https://perma.cc/P48Z-DHVJ>] describing technologies that use TSMC products).

320. *How TSMC Has Mastered the Geopolitics of Chipmaking*, THE ECONOMIST (Apr. 26, 2021), <https://www.economist.com/business/2021/04/29/how-tsmc-has-mastered-the-geopolitics-of-chipmaking> [<https://perma.cc/39ZJ-CU3L>].

321. See TSMC, *supra* note 316 (noting TSMC funding from the U.S. government).

322. *An Innovation Pioneer*, TSMC, <https://esg.tsmc.com/en-US/sustainability-roles/innovation-pioneer> [<https://perma.cc/J2X8-LAZK>] (last visited Sept. 16, 2024).

323. *Id.*

324. See U.S. DEP'T COM., *supra* note 95.

325. See, e.g., *Tsmc Is Exempted from China's Chip Export Ban for One Year to the United States: On the Condition That It Cannot Significantly Upgrade Its Technology*, UNWIRE.HK (Oct. 13, 2023) <https://unwire.hk/2023/10/13/tsmc-received-a-one-year-exemption-from-the-u-s-ban-on-chip-exports-to-china/life-tech/> [<https://perma.cc/TJZ5-5G9G>].

326. Sarah Wu & Ben Blanchard, *TSMC Expects Permanent U.S. Approval to Supply Chip Tools to its China Factory*, REUTERS (Oct. 13, 2023, 4:35 AM) <https://www.reuters.com/technology/taiwan-minister-says-tsmc-has-received-china-chip-waiver-extension-us-2023-10-13/> [<https://perma.cc/E7QY-7R3D>].

327. See *id.* (stating that the exception applies to a "less-advanced" facility in China).

328. UNWIRE.HK, *supra* note 325.

329. *Id.*

orchestration, and substantial investments in research and development, offering palpable benefits to the U.S. and the global semiconductor industry.<sup>330</sup>

### 3. *Problems of Major American Suppliers in Chip Manufacturing*

Substantial capital investments in research, development, and state-of-the-art manufacturing facilities constitute an imperative facet of the semiconductor industry.<sup>331</sup> While American semiconductor entities demonstrate considerable commitment, they allocate resources to a spectrum of operations, including chip design and research endeavors.<sup>332</sup>

The dominance of the ASML-TSMC nexus is sustained by the reluctance of American companies to enter into the chips' foundry services as well as the production of lithographic machines.<sup>333</sup> Prominent American semiconductor entities, including Intel, AMD, and Micron, confront notable impediments in their pursuit of manufacturing high-end chips comparable to those produced by TSMC.<sup>334</sup> These American firms face unique market demands and strategic priorities in exploring new skills and technologies, often enabling other companies to provide more cost-effective and specialized foundry services.<sup>335</sup> TSMC, through its concentrated efforts in semiconductor fabrication and substantial investments in technology and manufacturing capabilities, has attained a paramount position in the sphere of foundry-based high-end chip manufacturing.<sup>336</sup>

As it stands, TSMC's preeminence in semiconductor fabrication, cultivated over an extended period, epitomizes a pinnacle of technological acumen and operational finesse.<sup>337</sup> Their mastery of intricate manufacturing processes enables the production of chips with exceptional precision and operational efficiency.<sup>338</sup> TSMC's distinctive operational model, singularly devoted to semiconductor foundry services, stands in marked contrast to the multifaceted

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330. Samuel K. Moore, *Another Step Toward the End of Moore's Law: Samsung and TSMC Move to 5-Nanometer Manufacturing*, IEEE SPECTRUM (May 31, 2019), <https://spectrum.ieee.org/another-step-toward-the-end-of-moores-law> [<https://perma.cc/CSR8-A2AV>].

331. See SUTTER ET AL., *supra* note 72 ("These proposals sought to increase U.S.-based semiconductor fabrication and to address concerns about the adequacy of U.S. investment in research and development (R&D) and the development of the U.S. science and engineering workforce.").

332. *Id.*

333. Rokon Zaman, *ASML TSMC Nexus Fuels Semiconductor Monopoly*, THE WAVES (last updated Dec. 17, 2022), <https://www.the-waves.org/2022/03/25/asml-tsmc-nexus-fuels-semiconductor-monopoly/> [<https://perma.cc/F47Z-2LYD>].

334. See *The U.S.-China Chip War: Who Dares to Win?*, CITIGROUP (Jan. 2, 2024), <https://www.citigroup.com/global/insights/the-u-s-china-chip-war-who-dares-to-win> [<https://perma.cc/4NRF-TD9Z>] ("The former chair and CEO of the Taiwan Semiconductor Manufacturing Company (TSMC) . . . estimates that it would cost up to 50% more to make leading-edge chips in the U.S. than in Taiwan due to labor costs and different worker norms.").

335. *Id.*; see also Katie Canales, *The US Produces Just 12% of the World's Computer Chip Supply. Here's Why It's Trailing China When It Comes to Manufacturing and How it Plans to Get Ahead*, BUS. INSIDER (Apr. 17, 2021), <https://www.businessinsider.com/why-us-doesnt-make-chips-semiconductor-shortage-2021-4> [<https://perma.cc/MU2V-GS3V>] ("It became cheaper to build chip facilities in countries outside of the US.").

336. Zaman, *supra* note 333.

337. *Id.*

338. *Id.*

engagements of counterparts like Intel, AMD, and Micron.<sup>339</sup> The latter entities, spanning chip design, research, and development, allocate resources across a spectrum of industry facets.<sup>340</sup> While advantageous in certain contexts, this diversification potentially dilutes the singular focus necessary for the meticulous refinement of the manufacturing process.<sup>341</sup> In fact, the scale and scope of TSMC's semiconductor fabrication operations are of a magnitude seldom paralleled.<sup>342</sup> The extensive network of cutting-edge fabrication facilities facilitates handling large production volumes.<sup>343</sup> This colossal scale engenders economies of scale, resulting in cost-effective manufacturing processes.<sup>344</sup>

Regarding the development and production of chip-manufacturing machines, American companies face several hurdles in reproducing EUV lithographic machines akin to those manufactured by ASML.<sup>345</sup> The complexity of EUV lithography technology demands an extraordinary level of precision.<sup>346</sup> ASML's extensive experience, spanning decades, and its substantial patent portfolio underscore the intricacy involved.<sup>347</sup> Moreover, the substantial cost associated with EUV lithography machines presents a formidable barrier.<sup>348</sup> ASML's cutting-edge EUV machines command prices exceeding \$200 million each, a substantial capital outlay that American companies may find daunting.<sup>349</sup>

ASML's deep reservoir of highly skilled engineers and scientists specializing in EUV lithography technology gives them a distinct advantage. Competing with ASML regarding talent pool presents a formidable challenge for American counterparts. While a handful of American companies are endeavoring to develop their own EUV lithography machines, they remain in the nascent stages of development. It remains uncertain when they will achieve a level of sophistication comparable to ASML's offerings. In the interim, American semiconductor companies rely on ASML for their EUV lithography requirements. This dynamic bestows considerable market influence upon ASML and could render American semiconductor companies more susceptible to supply chain disruptions. In China, ASML has installed 1,400 DUV and

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339. Hille, *supra* note 318.

340. *See id.* (discussing how TSMC's business model differs from that of other companies).

341. *Id.*

342. *See id.* (discussing how the foundry model allowed TSMC to take over the market).

343. *See TSMC Holds 3nm Chip Ceremony in Taiwan, 2nm on Way, INSIDEHPC* (Jan. 2, 2023), <https://insidehpc.com/2023/01/tsmc-holds-3nm-chip-ceremony-in-taiwan-2nm-on-way/> [<https://perma.cc/UG5R-KBMS>] (“TSMC said that 3nm technology has successfully entered volume production with good yields, and held a topping ceremony for its Fab 18 Phase 8 facility. TSMC estimates that 3nm technology will create end products with a market value of US\$1.5 trillion within five years of volume production.”).

344. *See* Oliver Hamrin, *The Silicon Empire: TSMC's Revolution and Morris Chang's Legacy*, QUARTR (Aug. 27, 2024), <https://quatr.com/insights/company-research/the-silicon-empire-tsmcs-revolution-and-morris-changs-legacy> [<https://perma.cc/WZ3X-KD33>] (“One of the most hard-to-replicate competitive advantages of TSMC is the economies of scale established through decades of outpacing its competitors . . .”).

345. *Id.*

346. *Id.*

347. *Id.*; *see also* ASML Licenses Technology Patents to Intel, ASML (Feb. 23, 2005), <https://www.asml.com/en/news/press-releases/2005/asml-licenses-technology-patents-to-intel> [<https://perma.cc/QT67-JFG2>] (announcing a license agreement with Intel for “several lithography patents”).

348. Hamrin, *supra* note 344.

349. *Id.*

metrology machines.<sup>350</sup> China contributed 46% of ASML's system sales in 3Q23, while revenues in China grew 82% from the second quarter of 2023.<sup>351</sup>

In essence, the foundry service model underpinning TSMC's operations endows them with an enviable flexibility in manufacturing processes.<sup>352</sup> This adaptability is instrumental in accommodating the diverse array of high-end chips customarily sought by their clientele.<sup>353</sup> Transitioning from one generation of semiconductor manufacturing technology to the next presents a formidable undertaking.<sup>354</sup> This transition entails significant complexities and expenditures for entities like Intel, which traditionally focus on proprietary manufacturing processes.<sup>355</sup>

### C. Multiple Patterning

Traditional photolithography, the process of transferring circuit patterns onto a silicon wafer using light, faces physical limitations as feature sizes shrink.<sup>356</sup> This is where multiple patterning emerges as a critical technique for sustaining transistor scaling in modern chip manufacturing.<sup>357</sup> Multiple patterning is a technique used in semiconductor fabrication to create more complex and dense designs on computer chips.<sup>358</sup> It involves breaking down a single layer of patterns into multiple separate patterns that are printed in multiple passes using different masks.<sup>359</sup> By utilizing multiple patterning, manufacturers can achieve greater precision and improve the resolution of the final chip design.<sup>360</sup> This technique is essential for pushing the limits of semiconductor technology and enabling advancements in electronic devices.<sup>361</sup> At the heart of photolithography lies the wavelength of the light source used.<sup>362</sup> Currently, deep ultraviolet (DUV) light is the industry standard.<sup>363</sup> However, as feature sizes approach the wavelength of the light itself, the ability to define sharp patterns deteriorates.<sup>364</sup> Multiple patterning addresses this by breaking down the desired

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350. Judy Lin, *ASML Has Installed 1,400 DUV & Metrology Machines in China*, DIGITIMES ASIA (Nov. 3, 2023), <https://www.digitimes.com/news/a20231103VL204/asml-china-duv-ic-manufacturing-lithography-semiconductor-equipment.html> [<https://perma.cc/67G3-EV5H>].

351. *Id.*

352. Hamrin, *supra* note 344.

353. *Id.*

354. *Id.*

355. *Id.*

356. Zaman, *supra* note 333.

357. Hidetami Yaegashi et al., *Recent Progress on Multiple Patterning Process*, in 9051 ADVANCES IN PATTERNING MATERIALS AND PROCESSES XXXI 90510X-1 (Thomas I. Wallow & Christoph K. Hohle eds., 2014).

358. Anant Bhusal et al., *Multi-Material Digital Light Processing Bioprinting of Hydrogel-Based Microfluidic Chips*, BIOFABRICATION, Jan. 2022, at 1, <https://iopscience.iop.org/article/10.1088/1758-5090/ac2d78/pdf> [<https://perma.cc/9KTY-WFCC>].

359. *Id.* at 3.

360. David Z. Pan et al., *supra* note 29 (“Due to elongated delay of extreme ultraviolet lithography (EUVL), the semiconductor industry has been pushing the 193nm immersion lithography using multiple patterning to print critical features in 22nm/14nm technology nodes and beyond.”).

361. *Id.*

362. Zaman, *supra* note 333.

363. *Id.*

364. *Id.*

pattern into a series of steps, effectively bypassing the resolution limit of a single exposure.<sup>365</sup>

There are various multiple patterning techniques, each with its own complexity.<sup>366</sup> Double patterning (DP) is a fundamental example, where two masks and multiple lithography, deposition, and etch steps are used to create features smaller than the minimum resolution.<sup>367</sup> More complex techniques like triple or quadruple patterning involve even more steps, enabling the creation of even denser circuits.<sup>368</sup>

Multiple patterning offers significant advantages in the relentless pursuit of transistor miniaturization.<sup>369</sup> It allows chipmakers to achieve feature sizes beyond the capability of single-exposure lithography, leading to denser and more powerful ICs.<sup>370</sup> However, this complexity comes at a cost. MP processes involve more steps, increasing manufacturing time and cost.<sup>371</sup> Additionally, ensuring accurate registration and minimizing defect formation across multiple patterning steps presents a significant challenge for chipmakers.<sup>372</sup>

Despite these challenges, multiple patterning based on DUV technology remains essential for the foreseeable future in China, given the American sanction for the import of EUV-related equipment to the nation.<sup>373</sup> As researchers continue to explore alternative lithography techniques like extreme ultraviolet (EUV) lithography, multiple patterning serves as a bridge, enabling the continued miniaturization of transistors.<sup>374</sup>

#### D. Particle Accelerator Technology and SSMB

In pursuing preeminence in chip manufacturing, China has embarked on an innovative initiative to revolutionize lithography technology.<sup>375</sup> This endeavor

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365. See Yijian Chen et al., *Technological Merits, Process Complexity, and Cost Analysis of Self-Aligned Multiple Patterning*, 8326 OPTICAL MICROLITHOGRAPHY XXV 64 (Will Conley ed., 2012) (“Spacer based self-aligned multiple patterning (SAMP) techniques potentially allow us to scale integrated circuits down to sub-10nm half pitch with no need of EUV lithography.”).

366. *Multiple Patterning*, SEMICONDUCTOR ENG’G, [https://semiengineering.com/knowledge\\_centers/manufacturing/patterning/multipatterning/](https://semiengineering.com/knowledge_centers/manufacturing/patterning/multipatterning/) [<https://perma.cc/W3WX-SANX>] (last visited Sept. 24, 2024).

367. See Hidetami Yaegashi et al., *Overview: Continuous evolution on double-patterning process*, in ADVANCES IN RESIST MATERIALS AND PROCESSING TECHNOLOGY XXIX 83250B-1 (Mark H. Somervell & Thomas I. Wallow eds., 2012) (describing how double patterning can be used to create smaller features).

368. SEMICONDUCTOR ENG’G, *supra* note 366.

369. *Id.*

370. Rani S. Ghaida, et al., *A Methodology for the Early Exploration of Design Rules for Multiple-Patterning Technologies*, in PROC. OF THE INT’L CONF. ON COMPUTER-AIDED DESIGN 50 (2012).

371. *Id.*

372. Gregory Haley, *Single Vs. Multi-Patterning Advancements for EUV*, SEMICONDUCTOR ENG’G (June 20, 2024), <https://semiengineering.com/single-vs-multi-patterning-advancements-for-euv/> [<https://perma.cc/MU8B-JEHY>].

373. See Alex W. Palmer, *‘An Act of War’: Inside America’s Silicon Blockade Against China*, N.Y. TIMES (July 12, 2023), <https://www.nytimes.com/2023/07/12/magazine/semiconductor-chips-us-china.html> [<https://perma.cc/385B-SFGK>] (discussing America’s silicon blockade against China).

374. Xiaobin Xu et al., *Multiple-Patterning Nanosphere Lithography for Fabricating Periodic Three-Dimensional Hierarchical Nanostructures*, 11 ACS NANO 10384, 10386 (2017).

375. Kumar Priyadarshi, *China to Challenge ASML with a Better Technology than EUV*, TECHOVEDAS (Sept. 25, 2023), <https://techovedas.com/china-to-challenge-asml-with-a-better-technology-than-euv/> [<https://perma.cc/UMX3-YWKG>], (“In the race for semiconductor chip manufacturing, China has embarked on

can significantly disrupt the industry, particularly for established players like ASML.<sup>376</sup> China strategically positions itself to establish an expansive chip manufacturing facility driven by a particle accelerator, presenting a formidable challenge to ASML's dominance.<sup>377</sup> This technological advancement holds the promise of being a transformative force capable of circumventing U.S. sanctions and propelling China into a pivotal role within the global chip supply chain.<sup>378</sup> The endeavor is diligently progressing with the construction of a pivotal particle accelerator, a critical milestone in realizing this cutting-edge technological paradigm.<sup>379</sup>

This initiative is notably characterized by its central emphasis on harnessing particle accelerators to generate a state-of-the-art laser source for driving lithography machines, an indispensable component in microchip production.<sup>380</sup> In contrast to conventional methodologies, the Chinese initiative aims to achieve localization of manufacturing processes while concurrently bolstering the capacity for high-volume, cost-effective chip production.<sup>381</sup> This will be facilitated by establishing an expansive manufacturing facility that houses multiple lithography machines close to a single accelerator, marking a distinctive departure from prevailing industry practices.<sup>382</sup>

At the core of this significant technological leap lies the pioneering Steady-State Microbunching (SSMB) theory, which leverages the energy charged particles emit during acceleration, effectively serving as an illumination source.<sup>383</sup> The SSMB technology can yield a notably narrow bandwidth, limited scattering angle, and a continuous, unadulterated Extreme Ultraviolet (EUV) light source.<sup>384</sup> Compared with ASML's current EUV technology, SSMB offers a more optimal light source, featuring higher average power and chip production

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a groundbreaking venture to revolutionize lithography technology by exploring novel avenues that could potentially disrupt the industry especially ASML.”)

376. *See id.* (“China is strategizing the establishment of an immense chip manufacturing facility propelled by a particle accelerator to challenge ASML.”).

377. *Id.*

378. *See id.* (“This technology could be a game-changer that outstrips US sanctions and make China a key player in the chip world.”).

379. *See id.* (“They’re actively pushing forward with the construction of a crucial particle accelerator to bring this cutting-edge technology to life.”).

380. *See id.* (“This initiative is focused on leveraging particle accelerators to create a cutting-edge laser source for lithography machines, a crucial component in microchip production.”).

381. *See id.* (“Unlike traditional approaches, the Chinese project aims to localize manufacturing and bolster high-volume, low-cost chip production by constructing a colossal factory housing multiple lithography machines around a single accelerator.”).

382. *See id.* (“It aims to construct an extensive facility consolidating numerous lithography machines around a central accelerator.”).

383. *See id.* (“At the core of this technological breakthrough is the innovative Steady-State Microbunching (SSMB) theory . . . .”); *see also* Chuanxiang Tang et al., *An Overview of the Progress on SSMB*, 60TH ICFA ADV. BEAM DYNAMICS WORKSHOP ON FUTURE LIGHT SOURCES 166 (2018), <https://accelconf.web.cern.ch/fls2018/papers/thp2wb02.pdf> [<https://perma.cc/H6M5-GZHE>].

384. *See* Priyadarshi, *supra* note 375. (“SSMB theory utilizes the energy released by charged particles during acceleration to act as a light source, resulting in a narrow bandwidth, small scattering angle, and continuous pure Extreme Ultraviolet (EUV) light.”).

output at a lower unit cost.<sup>385</sup> ASML creates an EUV source from laser-produced plasma, where strong laser pulses are projected onto liquid microdroplets of tin.<sup>386</sup>

While ASML places paramount emphasis on the miniaturization of chip manufacturing machinery, aligning with international trade imperatives, the Chinese initiative is centered on domestic production endeavors.<sup>387</sup> Its primary objective entails the establishment of an expansive facility that consolidates numerous lithography machines surrounding a central accelerator.<sup>388</sup> This progression bears the potential to facilitate cost-efficient mass production of chips, positioning China at the vanguard of industrializing advanced chips with 2nm or even less.<sup>389</sup>

### E. Technological Readiness and Infrastructure Requirements

The technological readiness and infrastructure requirements of multiple patterning involve advanced lithography tools, precise materials, and skilled personnel, whereas particle accelerators necessitate specialized facilities, powerful magnets, precise beam control systems, and skilled physicists and engineers to operate and maintain them.<sup>390</sup>

#### 1. Multiple Patterning

The implementation of multiple patterning in chip manufacturing requires a high degree of technological readiness and a well-established infrastructure.<sup>391</sup> Technological readiness refers to the capability of semiconductor fabrication facilities to execute the complex processes involved in multiple patterning with

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385. See *id.* (“Compared to the existing ASML EUV technology, SSMB, [C]hinese tech proves to be a superior light source. It offers higher average power and increased chip production while maintaining lower unit costs.”); see also Xiujie Deng et al., *Experimental Demonstration of the Mechanism of Steady State Microbunching*, 590 NATURE 576, 576 (Feb. 24, 2021) (“The steady-state microbunching (SSMB) mechanism has been proposed to generate high-repetition, high-power radiation at wavelengths ranging from the terahertz scale to the extreme ultraviolet.”).

386. *Lights and Lasers*, ASML, <https://www.asml.com/en/technology/lithography-principles/light-and-lasers> [<https://perma.cc/2YQR-HMSS>] (last visited Sept. 21, 2024).

387. See Priyadarshi, *supra* note 375 (“ASML prioritizes downsizing chip manufacturing machines for international trade. In contrast, the Chinese initiative centers on domestic production.”); see also Chang Che & John Liu, *‘De-Americanize’: How China Is Remaking Its Chip Business*, N.Y. TIMES (May 11, 2023), <https://www.nytimes.com/2023/05/11/technology/china-us-chip-controls.html> [<https://perma.cc/B5PX-G6NM>] (discussing China’s effort to increase domestic production of computer chips).

388. See Priyadarshi, *supra* note 375 (“It aims to construct an extensive facility consolidating numerous lithography machines around a central accelerator.”).

389. *Id.*

390. See John Boyd, *Is the Future of Moore’s Law in a Particle Accelerator?*, IEEE SPECTRUM (June 10, 2024), <https://spectrum.ieee.org/euv-fel> [<https://perma.cc/H6NL-DJXE>] (discussing the technology of using a particle accelerator to create chips); *How Does an Accelerator Work*, CERN, <https://home.cern/science/accelerators> [<https://perma.cc/CS7U-M6AX>] (last visited Sept. 24, 2024) (“Accelerators use electromagnetic fields to accelerate and steer particles. Radiofrequency cavities boost the particle beams, while magnets focus the beams and bend their trajectory.”); Haley, *supra* note 372 (“[A]dvanced manufacturing tools such as inverse lithography technology (ILT) are needed that can highly optimize the mask pattern to reduce the minimum size and spaces between circuit features on the wafer.”).

391. See SEMICONDUCTOR ENG’G, *supra* note 366 (describing the technology behind multiple patterning).

precision and reliability.<sup>392</sup> This readiness encompasses various aspects, including lithography equipment, photoresist materials, etching and deposition techniques, metrology tools, and process control systems.<sup>393</sup> Advanced lithography tools, such as immersion and extreme ultraviolet (EUV) lithography machines, are essential for achieving the high resolution and tight tolerances required for multiple patterning.<sup>394</sup> Moreover, the availability of sophisticated process control technologies is crucial for monitoring and optimizing each step of the multiple patterning process to ensure consistent and accurate patterning across wafers.<sup>395</sup>

In addition to technological readiness, multiple patterning in chip manufacturing necessitates a robust infrastructure to support its implementation.<sup>396</sup> This infrastructure includes not only the physical facilities and equipment but also the expertise and workforce required to operate and maintain them.<sup>397</sup> Semiconductor fabrication facilities, commonly known as fabs, must be equipped with cleanrooms with stringent environmental controls to minimize contaminants that could affect patterning accuracy.<sup>398</sup> Furthermore, a reliable supply chain for critical materials, such as photoresists and chemicals used in the multiple patterning process, is essential to ensure uninterrupted production.<sup>399</sup> Additionally, skilled engineers and technicians with expertise in multiple patterning techniques are necessary to troubleshoot issues, optimize processes, and drive continuous improvement.<sup>400</sup> Overall, the technological

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392. See Bier, *supra* note 178 (outlining the challenges of the semiconductor manufacturing process and the opportunities to overcome these challenges).

393. See Li & Timings, *supra* note 259 (discussing six “critical semiconductor manufacturing steps”).

394. See Iason Giannopoulos et al., *Extreme Ultraviolet Lithography Reaches 5 NM Resolution*, 16 NANOSCALE 15533, 15533 (2024) (describing the advancement in extreme ultraviolet lithography to deliver sub-10 nm resolution); see also Jeff Hecht, *Photonic Frontiers: Extreme-UV Lithography Struggles to Shrink chip Features*, LASER FOCUS WORLD (June 1, 2009), <https://www.laserfocusworld.com/lasers-sources/article/16551203/photonic-frontiers-extreme-uv-lithography-extreme-uv-lithography-struggles-to-shrink-chip-feature> [<https://perma.cc/P4CL-9LHM>] (“Shorter wavelengths promise higher resolution . . .” and “[s]uch short wavelengths mean tighter tolerances . . .”).

395. See Robert Clark et al., *Perspective: New Process Technologies Required for Future Devices and Scaling*, 6 APL MATERIALS 058203, 058203-1 (2018) (explaining how process technologies can be implemented to optimize the steps in semiconductor manufacturing).

396. See, e.g., Kurt Ronse, *Patterning Infrastructure Development for Advanced EUV Lithography: Continuing Dimensional Scaling Through EUV Lithography to Support Moore’s Law*, 2 IEEE ELECTRON DEVICES MAG. 35, 35 (2024) (advocating for construction of new lens for EUV lithography).

397. See Harald Bauer et al., *Semiconductor Design and Manufacturing: Achieving Leading-Edge Capabilities*, MCKINSEY (Aug. 20, 2020), <https://www.mckinsey.com/industries/industrials-and-electronics/our-insights/semiconductor-design-and-manufacturing-achieving-leading-edge-capabilities> [<https://perma.cc/9ZFH-G37Z>] (discussing the need for appropriate physical and workplace infrastructure in the semiconductor industry).

398. See *Chips & Cleanrooms: Building the Heart of the U.S. Semiconductor Industry*, DESIGNTEK CONSULTING GRP. (Dec. 4, 2023), <https://www.designtekconsulting.com/post/chips-cleanrooms-building-the-heart-of-the-u-s-semiconductor-industry> [<https://perma.cc/3A2J-VU47>] (describing what a cleanroom is and the requirements to prevent contamination).

399. See Bauer et al., *supra* note 397 (“[C]ompanies need flexible and resilient supply chains that can quickly adjust.”).

400. See generally Brendan Jay et al., *New Tactics for New Talent: Closing U.S. Semiconductor Labor Gaps*, MCKINSEY (May 10, 2024), <https://www.mckinsey.com/industries/semiconductors/our-insights/new-tactics-for-new-talent-closing-us-semiconductor-labor-gaps> [<https://perma.cc/9YQX-2XQN>] (outlining the need for talent in the U.S. semiconductor industry); DESIGNTEK, *supra* note 398 (“Compounding this problem

readiness and infrastructure requirements of multiple patterning underscore the significant investments and capabilities needed to adopt this advanced manufacturing technique in chip fabrication facilities.<sup>401</sup>

## 2. Particle accelerators

Particle accelerators share fundamental technological and infrastructural prerequisites regardless of type or purpose.<sup>402</sup> These common requisites encompass a robust power source, a vacuum system to ensure particle isolation, integrating magnetic fields for particle control, and implementing precise control systems for beam regulation.<sup>403</sup> Additionally, particle accelerators necessitate specialized equipment, such as particle detectors, beamline components, and experimental apparatus, tailored to their specific type and intended application.<sup>404</sup>

Technologically, particle accelerator technology is well-established, exemplified by the Large Hadron Collider (LHC), which achieves proton energies of 6.5 TeV.<sup>405</sup> Infrastructure demands, however, vary widely depending on the accelerator's scale and purpose.<sup>406</sup> Small accelerators can be accommodated in compact laboratories, while colossal installations like the LHC necessitate expansive subterranean tunnels and structures.<sup>407</sup>

The construction and operation costs of particle accelerators can be substantial.<sup>408</sup> For instance, the LHC entailed an expenditure of over \$8

is the difficulty of getting a steady supply of the special, high-quality materials needed to build these specialized areas.”).

401. See Bauer et al., *supra* note 397 (“[N]ew fabs and extensive R&D programs—essential for producing leading-edge technologies at high volumes—require billions in investment.”).

402. See *How Particle Accelerators Work*, DEP’T OF ENERGY (June 18, 2014), <https://www.energy.gov/articles/how-particle-accelerators-work> [<https://perma.cc/S45X-VCDS>] (describing how particle accelerators work and their components).

403. *Id.*

404. See, e.g., *How a Detector Works*, CERN, <https://home.web.cern.ch/science/experiments/how-detector-works> [<https://perma.cc/URX4-QDPP>] (last visited Sept. 23, 2024) (describing how a particle detector works); *Beamline*, CHEMEUROPE, <https://www.chemeurope.com/en/encyclopedia/Beamline.html> [<https://perma.cc/F6EE-6Y3S>] (defining beamlines); see also *Accelerator Facility*, U.S. DEP’T OF ENERGY (Aug. 1, 2014), [https://www.directives.doe.gov/terms\\_definitions/accelerator-facility](https://www.directives.doe.gov/terms_definitions/accelerator-facility) [<https://perma.cc/5S5V-RX6G>] (last visited Oct. 8, 2024) (“The term facilities includes injectors, targets, beam dumps, detectors, experimental halls, non-contiguous support and analysis facilities, experimental enclosures and experimental apparatus utilizing the accelerator, etc, regardless of where that apparatus may have been designed, fabricated, or constructed, including all systems, components and activities that are addressed in the Safety Assessment Document (SAD).”).

405. Cian O’Luanaigh, *First Successful Beam at Record Energy of 6.5 TeV*, CERN (Apr. 10, 2015), <https://home.cern/news/news/accelerators/first-successful-beam-record-energy-65-tev> [<https://perma.cc/9W54-BXXK>].

406. See Maxwell Bernstein, *Bringing Compact Particle Accelerators to Industry*, FERMILAB (Jan. 22, 2024), <https://news.fnal.gov/2024/01/bringing-compact-particle-accelerators-to-industry/> [<https://perma.cc/LHN6-ST25>] (describing a compact particle accelerator’s development and funding).

407. See *id.* (describing a compact particle accelerator); see also *The Large Hadron Collider*, CERN, <https://home.cern/science/accelerators/large-hadron-collider> [<https://perma.cc/QVA8-MZNX>] (last visited Sept. 23, 2024) (describing the Large Hadron Collider).

408. See Edwin Cartlidge, *Much Cheaper, Smaller Atom Smashers May Be on the Horizon*, SCIENCE (Aug. 29, 2018), <https://www.science.org/content/article/much-cheaper-smaller-atom-smashers-may-be-horizon> [<https://perma.cc/64C5-PMYR>] (“The world’s biggest atom smasher . . . cost[s] \$5 billion.”); KWAN-

billion.<sup>409</sup> Despite this, the benefits derived from particle accelerators, spanning fundamental scientific discoveries to myriad applications in medicine, industry, and beyond, are commensurately significant.<sup>410</sup>

Distinct types of particle accelerators, including linear accelerators, cyclotrons, and synchrotrons, exhibit varying technological and infrastructural demands.<sup>411</sup> Linear accelerators, characterized by a linear particle trajectory, possess comparatively straightforward design and construction processes commonly applied in medical contexts like cancer therapy.<sup>412</sup> Cyclotrons, inducing particles into a spiral path, entail more intricate design and construction, finding prevalence in research areas, notably nuclear physics.<sup>413</sup> Synchrotrons, guiding particles along a circular path, require even more sophisticated construction efforts yet achieve significantly higher energy levels, making them pivotal in research fields like imaging and battery research.<sup>414</sup> The infrastructure prerequisites for these accelerators differ, and linear accelerators can be relatively compact, while cyclotrons and synchrotrons necessitate sizable production facilities.<sup>415</sup>

Particle accelerator technology stands at the forefront of scientific advancement, serving diverse applications.<sup>416</sup> Despite substantial costs, particle accelerators' profound contributions and applications render them indispensable in modern scientific and technological pursuits.<sup>417</sup>

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LIU MA ET AL., VISUALIZATION HANDBOOK 919 (2005) (“The design, construction, and operation of particle accelerators are very expensive and involve large-scale effort by teams of scientists and engineers from various disciplines.”).

409. Adam Mann, *What is the Large Hadron Collider?*, LIVE SCIENCE (Apr. 25, 2022), <https://www.livescience.com/64623-large-hadron-collider.html> [<https://perma.cc/KRD2-KBN9>].

410. See Nikki Forrester, *CERN's Impact Goes Way Beyond Tiny Particles*, NATURE (Apr. 17, 2024), <https://www.nature.com/articles/d41586-024-01100-w> [<https://perma.cc/ES7K-ZY4S>] (“Over the past 70 years, technologies developed at CERN to tackle technical and computing challenges have been applied throughout the world.”).

411. Jo Lewis & Christine Darve, *Accelerators Are Everywhere, Perhaps Closer Than You Think...*, SCI. IN SCH. (Sept. 2, 2024), <https://www.scienceinschool.org/article/2024/accelerators-are-everywhere/> [<https://perma.cc/4TSW-S7GS>].

412. See *Treatment Techniques: Linear Accelerators*, U. FLA. COLL. MED., <https://radonc.med.ufl.edu/patient-care/technologies-and-resources/treatment-techniques/> [<https://perma.cc/Y4H4-379P>] (last visited Sept. 24, 2024) (“[A] variety of medical linear accelerators (LINACs) are used to provide patients with external beam radiation therapy.”).

413. See generally Mukesh K. Pandey and Timothy R. DeGrado, *Cyclotron Production of PET Radiometals in Liquid Targets: Aspects and Prospects*, 14 CURRENT RADIOPHARMACEUTICALS 325 (2021) (discussing research using cyclotrons in nuclear physics).

414. See Nathan Collins, *Synchrotrons, the Swiss Army Knives of Science*, SLAC, <https://www6.slac.stanford.edu/research/slac-science-explained/synchrotrons> [<https://perma.cc/YVX4-EBZP>] (last visited Sept. 24, 2024) (outlining how synchrotrons work and their uses).

415. See David Bruhwiler, *How Particle Accelerators Work: From Linac to Synchrotron*, RADIASOFT (Apr. 23, 2020), <https://www.radiasoft.net/blog/how-particle-accelerators-work-from-linac-to-synchrotron/> [<https://perma.cc/EC3W-N6QF>] (outlining the differences between accelerator types).

416. See Geometrante et al., *Industry and Accelerator Science, Technology, and Engineering - The Need to Integrate (Building Bridges)*, 13TH INT. PARTICLE ACC. CONF., at 1646 (“Particle accelerators have a wide potential to expand beyond their present boundaries; they are a unique tool to access the atomic and subatomic world with many applications in the medical, industrial, environmental, and security fields.”).

417. See Neil Sapra et al., *On-Chip Integrated Laser-Driven Particle Accelerator*, 367 SCIENCE 1, 1 (“Particle accelerators represent an indispensable tool in science and industry. However, the size and cost of conventional radio-frequency accelerators limit the utility and reach of this technology.”).

### F. Comparative Analysis with Conventional Manufacturing Processes

The comparative analysis with conventional manufacturing processes highlights the increased precision and capabilities of multiple patterning in chip manufacturing, whereas particle accelerators offer unique research opportunities in fundamental physics beyond the capabilities of traditional experimental methods.<sup>418</sup>

#### 1. Multiple patterning

Multiple patterning in chip manufacturing involves utilizing conventional lithographic technology with enhanced complexity and expertise to achieve finer feature sizes and increased circuit densities.<sup>419</sup> This technique divides the patterning process into multiple intricate steps, each demanding precise execution and advanced skills.<sup>420</sup> Rather than relying on a single exposure, multiple patterning segments the desired pattern into multiple exposures, contributing to the final layout.<sup>421</sup> Implementing multiple patterning demands a profound comprehension of lithographic principles and processes, along with advanced manufacturing capabilities.<sup>422</sup> Semiconductor manufacturers must deploy sophisticated equipment, specialized materials such as high-resolution lithography tools, photoresists with exceptional resolution, etchants with precise selectivity, and robust process control mechanisms.<sup>423</sup> Skilled engineers and technicians play a pivotal role in optimizing manufacturing processes, troubleshooting issues, and driving continuous improvements.<sup>424</sup> Overall, multiple patterning represents a significant advancement in semiconductor fabrication, requiring technical expertise, state-of-the-art equipment, and meticulous process control to achieve desired results.<sup>425</sup>

#### 2. Particle accelerators

Particle accelerators and extreme ultraviolet (EUV) light sources are pivotal components of lithography technology employed in chip fabrication.<sup>426</sup> Both technologies present distinct attributes, each carrying its own set of

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418. See discussion *infra* Part IV.F.1, 2 (discussing multiple patterning and particle accelerators capability to generate EUV light in the context of conventional manufacturing).

419. Xu et al., *supra* note 374, at 10385–86.

420. *Id.* at 10385, fig. 1.

421. Seung Hak Park et al., *Block Copolymer Multiple Patterning Integrated with Conventional ArF Lithography*, 6 *SOFT MATTER* 120, 120 (2010).

422. *Ibid.*

423. See Li & Timings, *supra* note 259 (describing the steps and technologies needed for semiconductor manufacturing).

424. See *What is the Role of a Semiconductor Process Engineer?*, INQUIVIX TECHN. (Nov. 16, 2023), <https://inquivixtech.com/semiconductor-process-engineer/> [<https://perma.cc/FXY4-7P36>] (describing the responsibilities and role of a semiconductor engineer).

425. Xu et al., *supra* note 374, at 10386; Park et al., *supra* note 421, at 120.

426. Li, *supra* note 423; see England et al., *supra* note 29, at 1 (“Acceleration of particles in photonic nanostructures fabricated using semiconductor manufacturing techniques and driven by ultrafast solid state lasers is a new and promising approach to developing future generations of compact particle accelerators.”).

advantages and drawbacks.<sup>427</sup> Particle accelerators possess the capability to generate EUV light directly or produce alternative light forms that subsequently give rise to EUV light.<sup>428</sup> These accelerators are distinguished by their immense power, enabling the creation of high-quality EUV light.<sup>429</sup> Nevertheless, they are characterized by substantial size and cost.<sup>430</sup>

In contrast, prevailing EUV light sources, as produced by ASML, primarily rely on laser-produced plasma (LLP) technology.<sup>431</sup> This approach yields relatively smaller and more cost-effective sources than particle accelerators.<sup>432</sup> However, they exhibit comparatively lower power and generate EUV light of slightly diminished quality.<sup>433</sup>

The choice between particle accelerators and EUV (laser-produced plasma) sources hinges on the specific requirements of the chip manufacturer.<sup>434</sup> If high power and superior light quality are paramount, an EUV (laser-produced plasma) is preferred.<sup>435</sup> Conversely, a particle accelerator light source proves more advantageous if considerations revolve around cost and size.<sup>436</sup> Presently, all EUV lithography machines utilized in chip manufacturing operations are based on LLP EUV sources.<sup>437</sup> However, several enterprises are actively engaged in the development of particle accelerator-based EUV lithography machines.<sup>438</sup> While still in their nascent stages, these machines hold the potential

427. See Sapra et al., *supra* text accompanying note 417, at 1; see generally Sharma et al., *supra* note 297, at 7–13 (discussing and analyzing extreme ultraviolet lithography).

428. See England et al., *Laser-Driven Structure-Based Accelerators: White Paper for Snowmass 2021 Topical Group AF06 - Advanced Acceleration Concepts*, ARXIV (Mar. 16, 2022), <https://arxiv.org/abs/2203.08981> [<https://perma.cc/KX6M-WZAA>] (“The difference in bunch charge and duration for optically accelerated electron beams also points to the potential for future light sources for generation of attosecond-scale pulses of extreme ultraviolet (EUV) or X-ray radiation...”).

429. See generally Alexander Brynes, *Accelerator-Based Light Sources Get a Boost*, 590 NATURE 556, 556 (2021) (discussing the levels of power different types of accelerator-based light sources produce).

430. See Sapra et al., *supra* text accompanying note 417, at 1.

431. See Ganjaboy S. Boltaev et al., *Resonance-Enhanced Harmonics in Mixed Laser-Produced Plasmas*, 1 PLASMA RSCH. EXPRESS 1, 1 (2019) (describing laser-produced plasmas technology); see also *Light and Lasers*, ASML, <https://www.asml.com/en/technology/lithography-principles/light-and-lasers> [<https://perma.cc/JYD2-8KZG>] (last visited Sept. 22, 2024) (“In our laser-produced plasma (LPP) source, molten tin droplets of around 25 microns in diameter are ejected from a generator at 70 meters per second.”).

432. See generally ASML, *supra* text accompanying note 431.

433. See John Boyd, *Is the Future of Moore’s Law in a Particle Accelerator?*, IEEE SPECTRUM (June 10, 2024), <https://spectrum.ieee.org/euv-fel> [<https://perma.cc/E78Y-NE55>] (“[LLP] all adds up to a highly complex process. And although it starts off with kilowatt-consuming lasers, the amount of EUV light that is reflected onto the wafer is just several watts. The dimmer the light, the longer it takes to reliably expose a pattern on the silicon.”).

434. See Brynes, *supra* text accompanying note 429, at 1; see also Sapra et al., *supra* text accompanying note 417, at 1.

435. See Brynes, *supra* text accompanying note 429, at 1.

436. See Sapra et al., *supra* text accompanying note 417, at 1.

437. Jan Van Schoot, *The Moore’s Law Machine: The Next Trick to Tinier Transistors is High-Numerical-Aperture EUV Lithography*, 60 IEEE SPECTRUM 44, 46 (2023) (“Perhaps the most essential of these machines performs extreme-ultraviolet (EUV) photolithography. EUV lithography, the product of decades of R&D, is now the driving technology behind the past two generations of cutting-edge chips, used in every top-end smartphone, tablet, laptop, and server in the last three years.”).

438. See Boyd, *supra* note 433 (discussing a group of researchers are exploring the use of a particle accelerator in EUV lithography).

to confer substantial benefits, notably in terms of elevated power and enhanced EUV light quality.<sup>439</sup>

In the foreseeable future, it is probable that particle accelerator-based EUV lithography machines will emerge as the dominant technology in chip manufacturing. China is spending billions of dollars on this technology.<sup>440</sup> Particle accelerators' superior power generation and EUV light quality capabilities underpin this projection.<sup>441</sup> Nonetheless, the widespread availability of particle accelerator-based EUV lithography machines is anticipated to materialize over the course of several years.<sup>442</sup> This transition is expected to usher in a new era in lithography technology and significantly impact the supply chain of chip fabrication.<sup>443</sup>

### *G. Potential To Revolutionize Chip Production Efficiency and Capabilities*

The potential to revolutionize chip production efficiency and capabilities lies in the advanced patterning precision of multiple patterning and the fundamental research capabilities of particle accelerators, which together enable the fabrication of smaller and more intricate semiconductor devices and drive innovation in semiconductor technology.<sup>444</sup>

#### *1. Multiple patterning*

Multiple patterning has the potential to revolutionize chip production efficiency and capabilities by enabling the fabrication of semiconductor devices with significantly smaller feature sizes and higher circuit densities.<sup>445</sup> This advanced manufacturing technique divides the patterning process into multiple intricate steps, allowing for the creation of finer and more complex patterns than traditional lithography methods alone can achieve.<sup>446</sup> By segmenting the desired pattern into multiple exposures, multiple patterning enhances the resolution and accuracy of semiconductor fabrication, paving the way for the development of more powerful and efficient electronic devices.<sup>447</sup> Moreover, this approach enables semiconductor manufacturers to keep pace with the relentless demand

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439. *Id.*

440. Shilov, *supra* note 248.

441. See Boyd, *supra* note 433 (discussing a group of researchers are exploring the use of a particle accelerator in EUV lithography and its possible benefits).

442. *Id.* ("This is more than enough to drive not one but many next-generation lithography machines simultaneously, pushing down the cost of advanced chipmaking.")

443. See Shilov, *supra* note 248 ("Compared to the prevalent ASML EUV method, SSMB boasts superior power and efficiency, potentially reducing chip production costs.")

444. See Park et al., *supra* note 421, at 120 ("Double patterning is a promising resolution enhancement technique widely used in conjunction with conventional photolithography."); see also Boyd, *supra* note 433 (discussing the research of particle accelerators in chip manufacturing).

445. Tao Zhang et al., *Multiple Patterning via Layout Decomposition Method for Directed Self-Assembly Lithography*, 22 J. MICRO/NANOPATTERNING, MATERIALS, & METROLOGY 043001, 043001 (2023).

446. David Z. Pan et al., *supra* note 29.

447. See Xu et al., *supra* note 374, at 10385, fig. 1 (showing the multiple steps and exposures); see also *id.* at 10386 ("To our knowledge, this degree of versatility and precision has not previously been reported for structures prepared via nanosphere lithography.")

for increased performance and functionality in electronic products.<sup>448</sup> By harnessing multiple patterning, chip production can achieve greater efficiency and scalability, driving innovation and unlocking new possibilities in various industries reliant on semiconductor technology.<sup>449</sup>

## 2. Particle accelerator

Introducing particle accelerator technology represents a transformative prospect for microchip manufacturing on several fronts.<sup>450</sup> Firstly, these accelerators have the capacity to expedite and refine semiconductor production compared to conventional methodologies.<sup>451</sup> This is attributable to their ability to generate highly focused beams of charged particles, facilitating precise modification of materials at a microscopic scale.<sup>452</sup> As an illustration, lithography techniques based on particle accelerators can fabricate patterns on semiconductor chips with features as diminutive as a few nanometers.<sup>453</sup>

Secondly, particle accelerator technology holds the promise of engendering novel materials and processes in microchip manufacturing.<sup>454</sup> For instance, it can be leveraged to create semiconductor materials of a new ilk, endowed with enhanced attributes like heightened conductivity or augmented resistance to radiation-induced damage.<sup>455</sup> Additionally, particle accelerators can drive the development of innovative doping techniques, which are instrumental in introducing impurities into semiconductor materials for tailored adjustments in their electrical properties.<sup>456</sup>

Furthermore, particle accelerator technology stands poised to ameliorate the cost efficiency of microchip production.<sup>457</sup> This stems from its potential to optimize semiconductor fabrication in relation to conventional methods.<sup>458</sup>

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448. Hua-Yu Chang & Iris Hui-Ru Jiang, *Multiple Patterning Layout Decomposition Considering Complex Coloring Rules and Density Balancing*, 36 IEEE TRANSACTIONS ON COMPUT. -AIDED DESIGN INTEGRATED CIR. & SYSS. 280, 280 (2017); see Park et al., *supra* note 421, at 120 (“We present block copolymer multiple patterning as an efficient and truly scalable nanolithography for sub-20 nm scale patterning, synergistically integrated with conventional ArF lithography.”).

449. See generally Chang & Jiang, *supra* note 448 (discussing the benefits of multiple patterning); see Xu et al., *supra* text accompanying note 374.

450. See generally Boyd, *supra* note 433 (“A group of researchers at the High Energy Accelerator Research Organization, known as KEK, in Tsukuba, Japan, is betting EUV lithography might be cheaper, quicker, and more efficient if it harnesses the power of a particle accelerator.”).

451. Tobia Romano et al., *Metal Additive Manufacturing for Particle Accelerator Applications*, 27 PHYSICAL REV. ACCELERATORS & BEAMS 054801-1, 054801-1 (2024).

452. Lars Wischmeier et al., *High-NA EUV Lithography Optics Becomes Reality*, 11323 EXTREME ULTRAVIOLET (EUV) LITHOGRAPHY XI 1132308-1, 1132308-10 (2020).

453. Charles Q. Choi, *Particle Accelerator on a Chip Hits Penny-Size*, IEEE SPECTRUM (Oct. 24, 2023), <https://spectrum.ieee.org/particle-accelerator-chip-sized> [<https://perma.cc/7N2S-9PFT>].

454. See Romano et al., *supra* note 451, at 054801-1 (“The development of novel designs for complex accelerator components with enhanced performance, incorporating structures such as drift tubes, vacuum connectors, and cooling channels, has required the adoption of advanced manufacturing routes involving several fabrication steps and highly skilled labor for precise machining and joining operations.”).

455. See generally Sergey V. Kutsaev, *Advanced Technologies for Applied Particle Accelerators and Examples of Their Use*, 66 TECH. PHYSICS 161, 161 (2021) (discussing radiation and conductivity in the context of particle accelerators).

456. See NASDAQ, *supra* text accompanying note 252.

457. Priyadarshi, *supra* note 375.

458. *Id.*

Moreover, it could enable the production of a fresh cohort of chips that are inherently more cost-effective to manufacture.<sup>459</sup> To illustrate, lithographic techniques hinging on particle accelerators might curtail the need for a profusion of masks in semiconductor production, thus leading to substantial cost reductions.<sup>460</sup>

The prospective advantages of particle accelerator technology for microchip manufacturing are profound, including the creation of chips with heightened performance, lowered production costs, and novel functionalities.<sup>461</sup>

Examples of particle accelerator technology applications in microchip manufacturing are ion implantation and directed self-assembly (DSA).<sup>462</sup> Ion implantation involves the use of particle accelerators to introduce ions into semiconductor materials.<sup>463</sup> This process can be harnessed to alter the electrical characteristics of semiconductor materials, enabling the creation of chips with enhanced performance.<sup>464</sup> For instance, ion implantation is instrumental in crafting semiconductor transistors' n-type and p-type regions.<sup>465</sup> Additionally, it is employed to dope semiconductor materials with specific impurities like boron and phosphorus, thereby modifying their electrical conductivity.<sup>466</sup>

Directed self-assembly (DSA) is an auspicious technological frontier in microchip manufacturing that leverages particle accelerators to guide the arrangement of molecules into predetermined patterns.<sup>467</sup> DSA has the potential to fabricate semiconductor chips featuring nanometer-scale attributes that surpass the capabilities of traditional lithography techniques.<sup>468</sup> Nevertheless, DSA is currently in its infancy, and many challenges exist that necessitate resolution before it can be widely adopted in microchip manufacturing.<sup>469</sup>

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459. See *id.* (stating that China's approach "can fuel abundant and cost-effective chip production").

460. Shilov, *supra* note 248 (explaining that the Chinese attempt at use a particle accelerator creates an EUV light source); Haley, *supra* note 372 (stating that single patterning uses fewer masks, leading to lower cost, and EUV advancements have made single patterning more feasible).

461. See Priyadarshi, *supra* note 375 (explaining that the particle accelerator technology can lead to advanced chips like 2nm chips, increases chip production while lowering unit costs, and "has the potential to unlock new horizons for . . . technological innovation").

462. See Frank Watt, et al., *Proton beam writing*, 10 MATERIALS TODAY 20, 22, 25 (2007) (stating that a "particle accelerator provides a stable beam of MeV ions" for P-beam, which is a "useful tool for . . . directed self-assembly").

463. Felch et al., *Ion Implantation for Semiconductor Devices: The Largest Use of Industrial Accelerators*, PROCEEDINGS OF PAC2013, at 740.

464. See *Advanced Ion Implantation Solutions*, SYENSQO, <https://www.syensqo.com/en/solutions-market/electronics/semiconductors/ion-implantation#> [<https://perma.cc/ZP3S-UQ6C>] (last visited Sept. 21, 2024), ("Ion implantation is a doping method used in semiconductors that introduces impurities into a semiconductor wafer, enabling conductivity.")

465. See Masayasu Tanjyo & Masao Naito, *History of Ion Implanter and Its Future Perspective*, 73 SEI TECH. REV. 22, 22 (2011) ("The P-layer is made by implanting an electrically positive dopant, such as boron ion, into silicon, while the N-layer is made by implanting an electrically negative dopant . . .").

466. See *Fundamentals: Doping n- and p-semiconductors*, HALBLEITER, <https://www.halbleiter.org/en/fundamentals/doping/> [<https://perma.cc/C53K-N47R>] (last visited Sept. 22, 2024) ("Two of the most important materials silicon can be doped with, are boron . . . and phosphorus.")

467. Yu Chen & Shisheng Xiong, *Directed Self-Assembly of Block Copolymers for Sub-10nm Fabrication*, 2 INT. J. OF EXTREME MFG. 1, 2 (2020).

468. *Id.* at 17, 30.

469. *Id.* at 2.

While particle accelerator technology is still in the nascent stages of development for microchip manufacturing, it harbors the potential to revolutionize the industry.<sup>470</sup> By enabling the creation of innovative materials, processes, and devices, particle accelerator technology could usher in a new era of semiconductor chips characterized by unprecedented performance and capabilities.<sup>471</sup>

#### *H. Implications of China's Particle Accelerator Technology on Chip Manufacturing*

Although China is highly competitive in producing cutting-edge technology, the nation's ability to master semiconductor production, crucial for the digital economy, has been a challenge.<sup>472</sup> The 2022 decision by the U.S. to halt semiconductor exports to China underscored the industry's vulnerability to geopolitical tensions.<sup>473</sup> In response, China experienced a 450% surge in imports of DUV lithography machines for circuit imprinting before Dutch export restrictions took effect.<sup>474</sup>

Despite years of government subsidies, concerns about trade restrictions prompted China to intensify efforts through various information innovation projects, aiming to replace foreign suppliers in semiconductor technology.<sup>475</sup> The government now encourages collaboration between local chipmakers and suppliers as a strategic response to trade wars, leading to a deepening semiconductor supply chain.<sup>476</sup> However, the question of whether China's semiconductor industry can truly rival its global counterparts remains.<sup>477</sup> Therefore, it is not surprising that China is investigating alternative methods to circumvent limitations on lithography machines, which are crucial in manufacturing microchips.<sup>478</sup> Researchers are establishing the groundwork for the next frontier in semiconductor production by harnessing particle accelerators to generate an innovative laser source.<sup>479</sup>

To achieve nano-chip fabrication, China employs the technique of multiple patterning by using DUV lithography machines.<sup>480</sup> While DUV lithography, typically used for larger chips (14nm and above), relies on deep ultraviolet light

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470. England et al., *supra* note 29.

471. See Priyadarshi, *supra* note 375 (pointing out that particle accelerator technology “opens doors to new chip manufacturing approaches,” can be applied to other disciplines, and can lead to advanced 2nm chips).

472. *China is Quietly Reducing Its Reliance on Foreign Chip Technology*, THE ECONOMIST (Feb. 13, 2024), <https://www.economist.com/business/2024/02/13/china-is-quietly-reducing-its-reliance-on-foreign-chip-technology> [<https://perma.cc/KY7U-85H4>].

473. *Id.*

474. *Id.*

475. *Id.*; Jeff Pao, *SMIC to Sell Huawei Costly, Inefficient 5nm Chips*, ASIA TIMES (Feb. 8, 2024), <https://asiatimes.com/2024/02/smic-to-sell-huawei-costly-inefficient-5nm-chips/> [<https://perma.cc/7EXF-ULJD>].

476. THE ECONOMIST, *supra* note 472.

477. *Id.*

478. Shilov, *supra* note 248.

479. *Id.*

480. See *id.* (“This design aims to enable competitive manufacturing processes (such as 2nm and beyond) that will be used to make high-performance chips without using traditional extreme ultraviolet (EUV) lithography scanners.”).

to etch circuit patterns onto silicon wafers, multiple patterning overcomes its limitations for features like 7nm transistors.<sup>481</sup> This approach involves exposing the chip to DUV light multiple times, with each exposure creating a specific portion of the final circuit design.<sup>482</sup> By meticulously combining these partial patterns, they can achieve the desired feature size of 7nm.<sup>483</sup> However, this technique comes with drawbacks.<sup>484</sup> Multiple patterning significantly increases the number of production steps, making it more complex and expensive compared to the next-generation EUV lithography.<sup>485</sup> In essence, China's use of multiple patterning with DUV allows them to produce smaller chips, but at the cost of higher complexity, lower yield, and limited potential for further miniaturization.<sup>486</sup>

Particle accelerator technology possesses the capacity to enact a paradigm shift in chip manufacturing across various dimensions.<sup>487</sup> Primarily, it avails the opportunity to engender novel lithography tools.<sup>488</sup> Traditionally, lithography, the process of transferring a circuit pattern onto a wafer, relies on ultraviolet (UV) light.<sup>489</sup> However, particle accelerators have the capability to generate beams of charged particles, characterized by markedly greater precision and potency compared to UV light.<sup>490</sup> This augmentation in precision holds the potential to facilitate the production of chips with smaller features and more intricate designs.<sup>491</sup>

Furthermore, particle accelerator technology has the potential to yield innovations in materials and processes for chip manufacturing.<sup>492</sup> By way of illustration, particle accelerators can be instrumental in creating novel transistor configurations and other semiconductor devices.<sup>493</sup> Additionally, they offer

481. Nir Kshetri, *The Economics of Chip War: China's Struggle to Develop the Semiconductor Industry*, COMPUT., at 102 (June 2023). See Che-Jen Wang, *China's Semiconductor Breakthrough*, THE DIPLOMAT (Aug. 20, 2022), <https://thediplomat.com/2022/08/chinas-semiconductor-breakthrough/> [<https://perma.cc/RDQ6-YEGT>] (describing China's use of multiple patterning).

482. See Park, et al., *supra* note 421, at 121 ("Conventional double patterning requires multiple cycles of exposing and etching steps.").

483. See Wang, *supra* note 481 (explaining that using multiple patterning has been used for 7nm production).

484. See Haley, *supra* note 372 ("One of the primary challenges with high-NA EUV is the development of suitable resist materials, primarily metal oxides . . . . While metal oxide resists offer improved performance at smaller nodes due to their higher resolution and sensitivity, they are not yet ready for mass production.").

485. See Wang, *supra* note 481 ("[u]sing DUV machines requires more layers of masks, which means more times of exposure and more complexity. This will lead to a lower yield rate and a higher cost for each chip, making such a process commercially inviable nowadays.").

486. Jiann-Chyuan Wang & Yu-Chun Ma, *The Impact of Semiconductor's Technology Regulations from the U.S., Japan, and the Netherlands on China's Economy*, 18 TAIWAN STRATEGISTS 1, 10 (2023); Wang, *supra* note 481.

487. Priyadarshi, *supra* note 375.

488. *Id.*

489. Mike Murphy, *Why We Need EUV Lithography for the Future of Chips*, IBM (June 26, 2023), <https://research.ibm.com/blog/what-is-euv-lithography> [<https://perma.cc/2SBM-WEG3>].

490. E.J.N. WILSON, AN INTRODUCTION TO PARTICLE ACCELERATORS 201 (2001).

491. *Id.*

492. See Shilov, *supra* note 248 (stating that China's particle accelerator aims to enable manufacturing processes that do not use traditional EUV); ABACHY SEMICONDUCTOR MATERIALS AND EQUIP., *supra* note 254.

493. See Wang Jie, *China's Chipmaking Breakthrough Too Good to Be True*, CAIXIN GLOB. (Sept. 28, 2023), <https://www.globalneighbours.org/chinas-chipmaking-breakthrough-too-good-to-be-true/>

avenues for refining techniques for material deposition and etching on wafers.<sup>494</sup> This, in turn, may culminate in the production of chips characterized by heightened speed, efficiency, and durability.<sup>495</sup>

The advent of particle accelerator technology has profound implications for global chip manufacturing. This entails the prospect of fabricating chips with minuscule feature sizes, thus affording enhanced potency and complexity.<sup>496</sup> Furthermore, the technological advances facilitated by particle accelerators are poised to usher in a new era of chip performance and reliability.<sup>497</sup> It is incumbent upon the research and development community to explore and harness the full potential of this nascent frontier, heralding a future of smaller, swifter, more efficient, and more dependable chips.<sup>498</sup>

#### V. LIMITATIONS OF BOTH CHIPS ACTS IN BOOSTING LOCAL CHIP MANUFACTURING

The CHIPS Act and the EU Chips Act, enacted in the U.S. and Europe, respectively, represent a legislative initiative aimed at bolstering domestic semiconductor manufacturing and research endeavors.<sup>499</sup> However, it appears that these acts demonstrate inefficacy when applied to the domain of particle accelerator chip production, primarily due to their failure to align with the nuanced exigencies of this nascent and specialized technology.<sup>500</sup>

Central to the challenges inherent in particle accelerator chip manufacturing is the imperative for an exceptionally elevated degree of precision and accuracy.<sup>501</sup> This necessitates strict regulating of particle beams

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[<https://perma.cc/F92T-EGUZ>] (explaining that the smaller the transistor, the more that can fit on a chip, and “Chinese scientists have supposedly created a new source for EUV light” for this process.)

494. *See id.* (stating that Chinese scientists claim they have created a new source for EUV light through using a particle accelerator to etch wafers).

495. *See* Priyadarshi, *supra* note 375 (explaining that using a particle accelerator “offers higher average power and increased chip production while maintaining lower unit costs” and could “make China a key player in the chip world”).

496. *See* Jie, *supra* note 493 (“Semiconductor sophistication is measured in nanometers, indicating the size of the transistors—the smaller they are the more can fit onto a chip.”).

497. *See* Ben Hernandez, *Particle Accelerators Could Make China Semiconductors Leader*, VETTAFI (Sept. 29, 2023), <https://www.etftrends.com/china-insights-channel/particle-accelerators-could-make-china-semiconductor-leader/> [<https://perma.cc/5T9Y-ZP2K>] (“The use of particle accelerators could aid in producing more chips for AI usage. This would help make China a world leader in the semiconductor manufacturing industry.”).

498. *See generally*, THE WHITE HOUSE, *supra* note 67 (discussing the importance of further research and development in the field of semiconductors and microchips); *see also* Hernandez, *supra* note 497 (reporting on China’s foray into particle accelerator chip manufacturing).

499. THE WHITE HOUSE, *supra* note 15; EUR. COMM’N, *supra* note 25.

500. Laurie E. Locascio, *Update on CHIPS Act implementation*, 12496 SPIE (2023); CHIPS and Science Act, Pub. L. No. 114-167, §§ 10106, 10109, 136 Stat. 1366.

501. *Particle Accelerators Cut Silicon: A Fascinating Process*, FINDLIGHT (May 31, 2023), <https://www.findlight.net/blog/particle-accelerators-cut-silicon-a-fascinating-process/> [<https://perma.cc/Y7R4-G5WV>]; *see generally* John Wallace, *Laser-Based Microchip Particle Accelerator Can Benefit Industry and Medicine*, LASER FOCUS WORLD (Nov. 26, 2018), <https://www.laserfocusworld.com/lasers-sources/article/16571391/laser-based-microchip-particle-accelerator-can-benefit-industry-and-medicine> [<https://perma.cc/G9F2-2MWV>] (“One of the challenges is that the vacuum channel for the electrons on a chip has to be made very small, which requires that the electron beam be extremely focused.”).

within particle accelerators and instruments leveraged across a diverse array of scientific and industrial applications.<sup>502</sup>

While the CHIPS Act and the EU Chips Act allocate resources toward research and development within the ambit of semiconductor manufacturing, they lack provisions directly addressing the singular challenges intrinsic to particle accelerator chip production.<sup>503</sup> Financial backing for cultivating specialized apparatus and tools requisite to this specialized domain is absent.<sup>504</sup>

Furthermore, the legislative focus of the CHIPS Act and the EU Chips Act predominantly gravitates toward the advancement of conventional semiconductor manufacturing technologies.<sup>505</sup> In contradistinction, particle accelerator chip manufacturing constitutes an incipient technological frontier wherein the long-term viability of various technological paradigms remains uncertain.<sup>506</sup> Consequently, the CHIPS Act and the EU Chips Act fall short of providing adequate support for the progression of particle accelerator chip manufacturing within the U.S.<sup>507</sup> This situation urgently calls for the government to administer more targeted and specific support for this emerging technological frontier.<sup>508</sup>

#### A. *Analyzing the Limitations on Funding*

The CHIPS Act and the EU Chips Act face significant limitations inherent to their funding allocation that may impact their efficacy.<sup>509</sup> One notable constraint is the extended duration over which the funding is apportioned, spanning a period of a number of years.<sup>510</sup> This protracted timeline implies that the full ramifications of the funding infusion may not be expeditiously discernible.<sup>511</sup>

It is worth noting that the CHIPS Act and the EU Chips Act, with some substantial financial commitment, do not comprehensively address all the challenges confronting the semiconductor industry.<sup>512</sup> For instance, neither act

502. FINDLIGHT, *supra* note 501; *see also* M. Gasior et al., *Introduction to Beam Instrumentation and Diagnostics*, in PROCEEDINGS OF THE CAS-CERN ACCELERATOR SCHOOL: ADVANCED ACCELERATOR (W. Herr eds, 2014) (discussing particle accelerator diagnostics including beam and particle measurements and positioning).

503. CHIPS and Science Act, Pub. L. No. 114-167, §§ 10106, 10109, 136 Stat. 1366; THE WHITE HOUSE, *supra* note 15.

504. *Id.*

505. *Id.*

506. Robin Mitchell, *China's Semiconductor War Response: Custom Particle Accelerator*, ELECTROPAGES (Sep. 29, 2023), <https://www.electropages.com/blog/2023/09/china-building-particle-accelerator-create-future-semiconductors> [<https://perma.cc/6T9K-QPKC>]; Hernandez, *supra* note 497.

507. Madeline Ngo, *CHIPS Act Funding for Science and Research Falls Short*, N.Y. TIMES (May 30, 2023) <https://www.nytimes.com/2023/05/30/us/politics/chips-act-science-funding.html> [<https://perma.cc/K4UH-DABP>].

508. *Id.*

509. Kannan & Feldgoise, *supra* note 119; EUR. COMM'N, *supra* note 25.

510. *Two Years Later: Funding from CHIPS and Science Act Creating Quality Jobs, Growing Local Economies, and Bringing Semiconductor Manufacturing Back to America*, U.S. DEP'T OF COM. (Aug. 9, 2024), <https://www.commerce.gov/news/blog/2024/08/two-years-later-funding-chips-and-science-act-creating-quality-jobs-growing-local> [<https://perma.cc/YSJ5-MKBC>].

511. *Id.*

512. Kannan & Feldgoise, *supra* note 119; Ngo, *supra* note 507.

earmarks funding for critical areas such as workforce development or the incubation of novel semiconductor technologies.<sup>513</sup> This implies that supplementary measures may be required to lend sustained support to the semiconductor industry in the long term.<sup>514</sup> Moreover, the dispersion of funding across diverse programs could potentially dilute the focus on the most promising technologies, such as particle accelerator chip manufacturing.<sup>515</sup>

A further limitation pertains to the stipulated constraints on the utilization of the funding as provided by both acts.<sup>516</sup> Notably, according to the CHIPS Act, entities receiving funding are proscribed from expanding semiconductor manufacturing activities in countries such as China, which are deemed to pose national security concerns to the U.S.<sup>517</sup> These restrictions may impede companies' capacity to attract investment and establish new semiconductor fabrication facilities.<sup>518</sup>

Notwithstanding these limitations, the CHIPS Act and the EU Chips Act embody a substantial investment in the semiconductor industry and harbor the potential to galvanize domestic manufacturing and research efforts.<sup>519</sup> It is, however, incumbent upon stakeholders to maintain a realistic appraisal of the constraints associated with the funding and to engage in ongoing assessment to ensure its alignment with intended objectives.<sup>520</sup>

Last but not least, it should be noted that emerging ventures in American chip manufacturing face persistent hurdles, including the escalating costs and delays associated with large-scale environmental assessments and labor union issues.<sup>521</sup> Current trends favoring unionized labor for federal contracts, coupled with a labor shortage, may impede chipmakers' talent acquisition and escalate

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513. THE WHITE HOUSE, *supra* note 15; EUR. COMM'N, *supra* note 25; *see also* Lucas Mearian, *Why Billions of CHIPS Act Dollars Have Not Been Distributed*, COMPUTERWORLD (Dec. 11, 2023), <https://www.computerworld.com/article/1611166/why-billions-of-chips-act-dollars-have-not-been-distributed.html> [<https://perma.cc/7HW6-E4CW>] (discussing the difficulties TSMC has had finding skilled labor and high-tech workers while noting Micron's investment in semiconductor student education and programs).

514. Kannan & Feldgoise, *supra* note 119.

515. *EU Funding Programmes*, EUR. COMM'N, [https://commission.europa.eu/funding-tenders/find-funding/eu-funding-programmes\\_en](https://commission.europa.eu/funding-tenders/find-funding/eu-funding-programmes_en) [<https://perma.cc/DA5Y-W6DW>] (last visited Sept. 23, 2024). *See* Lindsay McKenzie, *CHIPS Program Suspends Plans for R&D Facility Funds*, AIP (Apr. 1, 2024) <https://ww2.aip.org/fyi/chips-program-suspends-plans-for-r-d-facility-funds> [<https://perma.cc/9H9N-2Y3N>] (discussing CHIPS Act funding difficulties and demand).

516. 15 C.F.R. § 231.202.

517. *Id.*

518. *Id.*; Sujai Shivakumar et al., *supra* note 108 (“In short, these reactions suggest that the current language and especially the thresholds envisaged for the proposed guardrails appear to be too stringent and may well be counterproductive in terms of global supply and the health of the global supply chain, ultimately undermining U.S. policy objectives.”).

519. THE WHITE HOUSE, *supra* note 15; EUR. COMM'N, *supra* note 25.

520. *See* 15 C.F.R. § 231.202 (“No later than the date of the award of Federal financial assistance award under 15 U.S.C. 4652, the covered entity shall enter into a required agreement that contains this prohibition and otherwise implements the requirements of this part.”).

521. *See* Veronique de Rugy, *The CHIPS Act Is Corporate Welfare Disguised as Industrial Policy*, REASON (July 28, 2022, 12:01 AM), <https://reason.com/2022/07/28/the-chips-act-is-corporate-welfare-disguised-as-industrial-policy/> [<https://perma.cc/U6PJ-MYU5>] (“Any resulting new operations would still face deep-rooted issues hindering American manufacturing. Large-scale environmental assessments will be required, but over the years, the costs and delays have become excessive.”).

domestic production costs.<sup>522</sup> The funding provided by the CHIPS Act can hardly address these fundamental and critical cost and labor issues.<sup>523</sup>

*B. Analyzing the Limitations on Semiconductor Manufacturing Locations*

The CHIPS Act, a decisive legislative framework in the U.S., strategically imposes a series of constraints with regard to the geographic locations of semiconductor manufacturing.<sup>524</sup> These measures are primarily motivated by imperatives pertaining to national security and the assurance of a dependable semiconductor supply chain within the nation.<sup>525</sup>

One prominent constraint within the ambit of the CHIPS Act stipulates that entities receiving funding must refrain from augmenting semiconductor manufacturing operations in nations identified as posing a national security threat to the U.S., notably China.<sup>526</sup> This restriction introduces potential complexities for companies seeking investment and establishing new semiconductor fabrication facilities in these designated regions.<sup>527</sup>

Another critical constraint mandates that entities benefiting from CHIPS Act funding must maintain a prescribed threshold of semiconductor manufacturing activity within the U.S.<sup>528</sup> This requisition is expressly designed to safeguard the existence of a domestic supply of semiconductors, particularly in the event of disruptions to the global supply chain.<sup>529</sup> Furthermore, the Act compels recipient companies to furnish comprehensive information pertaining to their semiconductor manufacturing operations.<sup>530</sup> This provision is strategically crafted to provide the government with a clear and comprehensive overview of the semiconductor supply chain.<sup>531</sup> It also serves to enable the identification and mitigation of potential risks.<sup>532</sup>

The prescribed limitations on semiconductor manufacturing locations within the CHIPS Act have evoked diverse reactions.<sup>533</sup> Advocates assert that these restrictions are indispensable in safeguarding national security interests

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522. *Id.*

523. *See id.* (“[B]elieving that these subsidies will promote our national security by helping companies relocate production to the United States is rooted in faith rather than facts.”).

524. 15 C.F.R. § 231.202; *See* Tom Dworetzky, *Where the CHIPS Act is Transforming the US Semiconductor Ecosystem*, CAMOIN ASSOCIATES (Oct. 3, 2023) <https://camoinassociates.com/resources/chips-act-is-transforming-the-us-semiconductor-ecosystem/> [<https://perma.cc/52S4-2YJT>] (noting Arizona, Texas, New York, Ohio, Idaho, and Utah are the states receiving the top funding).

525. THE WHITE HOUSE, *supra* note 15.

526. *Id.*

527. *Id.*

528. *Id.*

529. PWC, *supra* note 85; Sutter et al., *supra* note 72.

530. BLEVINS ET AL., *supra* note 38, at 1–4 (discussing the requirements and restrictions related to the America Fund under the CHIPS Act).

531. *Ibid.*

532. *Ibid.*

533. *See, e.g.*, Rugsy, *supra* note 521 (“[B]elieving that these subsidies will promote our national security by helping companies relocate production to the United States is rooted in faith rather than facts.”); Kannan & Feldgoise, *supra* note 119.

and ensuring an assured supply of semiconductors within the U.S.<sup>534</sup> Conversely, detractors argue that the constraints may be overly prohibitive, potentially impeding the competitiveness of companies within the global semiconductor arena.<sup>535</sup>

The implications of these constraints within the CHIPS Act are far-reaching. While it remains too early to ascertain their long-term ramifications conclusively, they are poised to induce substantive shifts in the methodologies employed for semiconductor production and distribution.<sup>536</sup> This could potentially lead to reduced investments directed towards semiconductor manufacturing in nations, notably China, which is identified as a national security concern to the U.S., potentially resulting in increased operational costs for semiconductor firms.<sup>537</sup>

In contrast, while not expressly delineating restrictions on semiconductor manufacturing locations, the EU Chips Act introduces provisions that may indirectly influence the decisions of semiconductor companies regarding the locales of their factories.<sup>538</sup> Specifically, the Act introduces financial incentives to encourage semiconductor firms to establish manufacturing facilities within the boundaries of the EU.<sup>539</sup> This provision could potentially render Europe a more enticing option for companies, even if their initial preference might have leaned towards alternative global locations.<sup>540</sup> Moreover, the Act encompasses measures designed to fortify the European semiconductor supply chain.<sup>541</sup> This could result in heightened reliance on suppliers within the EU, potentially rendering it more challenging for semiconductor companies to continue their reliance on suppliers beyond the EU's borders.<sup>542</sup>

Overall, the CHIPS Act and EU Chips Act are poised to influence semiconductor manufacturing positively within the U.S. and Europe.<sup>543</sup>

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534. *Biden-Harris Administration Announces Final National Security Guardrails for CHIPS for America Incentives Program*, NIST (Sept. 22, 2023), <https://www.nist.gov/news-events/news/2023/09/biden-harris-administration-announces-final-national-security-guardrails> [<https://perma.cc/2B92-XQSB>].

535. Shivakumar et al., *supra* note 108.

536. *Id.*

537. *Id.*

538. EUR. COMM'N, *supra* note 25.

539. *See The Impact of the European Chips Act on Global Technology Markets*, INNOVATION NEWS NETWORK (Nov. 16, 2023) <https://www.innovationnewsnetwork.com/the-impact-of-the-european-chips-act-on-global-technology-markets/39998/> [[perma.cc/HK5Y-CW77](https://perma.cc/HK5Y-CW77)] (“Furthermore, strategic investments by international tech giants such as Intel are expected within EU territories due to this legislative push. Introducing innovation and competence centres also forms part of this comprehensive approach to redefining global technology markets.”).

540. *See id.* (“The Act’s broad-reaching implications include facilitating SMEs’ growth, enabling new semiconductor plant constructions across member states, spurring job creation, and regional economic development.”).

541. *See id.* (“These comprehensive strategies are expected to contribute meaningfully towards reducing dependency on non-EU nations for semiconductors while enhancing supply chain security.”).

542. *Id.*

543. *See* Sujai Shivakumar et al., *supra* note 28 (“Both pieces of legislation envision industry-government partnerships with similar strategic goals: reducing dependency on offshore chip manufacturing, ensuring greater supply chain security and resiliency, encouraging production at the leading edge, and growing a workforce to support the achievement of these goals.”).

However, it is imperative to underscore that these acts may significantly impact the geographic placement of semiconductor factories in the U.S. and Europe.<sup>544</sup>

## VI. RECOMMENDATIONS TO IMPROVE THE CHIPS ACT

The CHIPS Act constitutes an important legislative endeavor directed toward fortifying and consolidating the semiconductor industry in the U.S.<sup>545</sup> Possible areas that may require reconsideration encompass augmented financial allotments, the enlargement of eligibility parameters, an intensified focus on research endeavors, and the implementation of safeguards pertaining to labor.<sup>546</sup> Integral to this endeavor is the imperative of addressing national security imperatives and affording due support to nascent technologies, exemplified by incorporating particle accelerator methodologies.<sup>547</sup>

In order to maximize the Act's efficacy, prudent contemplation of amendments is required. These may encompass a reinforced allocation of resources earmarked for Research and Development, concomitant with the institution of tax incentives designed to incentivize private sector engagement.<sup>548</sup> Concurrently, the cultivation of collaborative alliances with educational institutions and the formulation of a holistic national strategy germane to the semiconductor domain emerge as imperatives for sustained viability over the long term.<sup>549</sup> These measures are strategically poised to

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544. See, e.g., Sarah Kreps & Paul Timmers, *Bringing Economics Back into EU and U.S. Chips Policy*, BROOKINGS INST. (Dec. 20, 2022), <https://www.brookings.edu/articles/bringing-economics-back-into-the-politics-of-the-eu-and-u-s-chips-acts-china-semiconductor-competition/> [perma.cc/N3BX-RMRT] (“Yet those goals need not be realized through protectionist policies; indeed, they may be undercut by them.”).

545. See THE WHITE HOUSE, *supra* note 15 (“It will strengthen American manufacturing, supply chains, and national security, and invest in research and development, science and technology, and the workforce of the future to keep the United States the leader in the industries of tomorrow, including nanotechnology, clean energy, quantum computing, and artificial intelligence.”); Shivakumar et al., *supra* note 28.

546. See generally *FACT SHEET: Biden-Harris Administration Announces Over \$5 Billion from the CHIPS and Science Act for Research, Development, and Workforce*, THE WHITE HOUSE (Feb. 9, 2024), <https://www.whitehouse.gov/briefing-room/statements-releases/2024/02/09/fact-sheet-biden-harris-administration-announces-over-5-billion-from-the-chips-and-science-act-for-research-development-and-workforce/> [https://perma.cc/EM3D-2TMX] (discussing the details of the CHIPS Act). See, e.g., Ross & Muro, *supra* note 90; Chris M. Rodrigo, *Leveraging the CHIPS Program to Create Good Jobs for All Semiconductor Workers*, INST. FOR POL’Y STUD. (Aug. 22, 2024), <https://ips-dc.org/report-leveraging-chips-program-to-create-good-jobs/> [https://perma.cc/68ZE-GMYT].

547. See, e.g., *National Security*, NIST (last updated Dec. 19, 2023), <https://www.nist.gov/chips/national-security> [perma.cc/4SDX-HVDW] (“To strengthen U.S. national security, CPO seeks projects that expand or modernize the production of chips that serve U.S. national security missions while also serving commercial markets.”); Ross & Muro, *supra* note 90 (“The national security establishment knows last year’s \$250 billion CHIPS and Science Act mostly for its bold subsidies to encourage firms to build new semiconductor plants and thus compete with China on industrial strategy.”).

548. See THE WHITE HOUSE, *supra* note 15 (discussing current Research and Development funding and tax incentives).

549. See, e.g., Matthew Schleich, *Securing Semiconductors: How to Scale-up Global Semiconductor Production and Protect U.S. National Security at the Same Time*, DEP’T OF STATE (May 15, 2023), <https://www.state.gov/securing-semiconductors-how-to-scale-up-global-semiconductor-production-and-protect-u-s-national-security-at-the-same-time/> [perma.cc/Z73Q-N95Q] (“The passage of the CHIPS Act gave the opportunity for the State Department to implement \$500 million over the next five years to enhance international security and resilience in key technology sectors.”); Jon Barnhart, *What the CHIPS and Science Act Means for Higher Education*, EAB (Sept. 12, 2022), <https://eab.com/resources/blog/strategy-blog/what-chips-science-act-means-higher-education/> [https://perma.cc/Z38G-R4JS].

diminish dependency upon foreign suppliers and uphold the vanguard position of the U.S. within the sphere of semiconductor technology.<sup>550</sup> Successful implementation, however, mandates the promulgation of lucid guidelines and the expeditious and judicious administration of the abovementioned provisions.<sup>551</sup>

A. *How Theories Can Explain the Shortcomings of the CHIPS Act*

Appropriate analytical frameworks such as disruptive innovation and path dependency can offer valuable perspectives in examining the ramifications of the CHIPS Act.<sup>552</sup> These theoretical constructs furnish a structured lens through which one may comprehend both the obstacles and prospects entailed in the assimilation of novel technologies.

1. *Disruptive Innovation Theory*

One theoretical framework elucidating the reluctance of American companies to embrace novel technologies, particularly when their extant enterprises are intricately intertwined with established technological paradigms, is the disruptive innovation theory.<sup>553</sup> This conceptual framework, pioneered by Clayton Christensen and his colleagues, expounds upon how emergent technologies possess the capacity to engender perturbations within extant markets and industries.<sup>554</sup>

Disruptive innovations represent promising technological advancements characterized by an altered value proposition relative to established technologies.<sup>555</sup> These innovations may be distinguished by attributes such as enhanced cost-effectiveness, heightened convenience, or enhanced usability.<sup>556</sup>

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550. See *Biden-Harris Administration Awards \$269M for Microelectronics Manufacturing and Workforce Development; Boosting U.S. Chip-Making Capabilities*, DEP'T OF DEF. (Sept. 17, 2024), <https://www.defense.gov/News/Releases/Release/Article/3908176> [perma.cc/RL2V-RX2Q] (“This investment is funded by the CHIPS and Science Act . . . aimed at strengthening the nation’s semiconductor manufacturing capabilities and reducing dependency on foreign sources of microelectronics.”); Jeffrey Kucik, *Dependencies in the US Semiconductor Industry*, WILSON CTR.: CTRL FORWARD (Mar. 28, 2024), <https://www.wilsoncenter.org/blog-post/dependencies-us-semiconductor-industry> [https://perma.cc/E972-QRZS].

551. See, e.g. Kannan & Feldgoise, *supra* note 119 (“The act is a major step forward, but it leaves multiple gaps that require additional government action.”); Jennifer Plitsch et al., *Biden Administration Announces Priorities for the Implementation of the CHIPS Act of 2022*, COVINGTON (Aug. 31, 2022), <https://www.insidegovernmentcontracts.com/2022/08/biden-administration-announces-priorities-for-the-implementation-of-the-chips-act-of-2022/> [https://perma.cc/2VN6-X7F8].

552. Ellie Gabel, *Disruptive Tech Transforming Chip Engineering*, EPSNEWS (May 2, 2024), <https://epsnews.com/2024/05/02/disruptive-technologies-transforming-semiconductor-engineering/> [https://perma.cc/RLQ9-L3AC]; Carolina Castaldi et al., *Path Dependence in Technologies and Organizations*, THE PALGRAVE ENCYCLOPEDIA STRATEGIC MGMT. 1256, 1257.

553. Clayton Christensen, et al., *What Is Disruptive Innovation*, HARV. BUS. REV. (Dec. 2015), <https://hbr.org/2015/12/what-is-disruptive-innovation> [https://perma.cc/WBL7-5MH4].

554. *Id.*

555. See Yu Dan and Hang Chang Chieh, *A Reflective Review of Disruptive Innovation Theory*, 12 INT’L J. MGMT. REVIEWS 402, 402 (2008) (“Disruptive Innovation is a powerful means for broadening and developing new markets and providing new functionality, which, in turn, may disrupt existing market linkages.”).

556. *Id.* at 404 (“Products based on disruptive technologies are typically simpler, cheaper, more reliable and convenient than established technologies from customers’ viewpoint.”).

Consequently, disruptive innovations can engender a realignment of customer preferences, often at the expense of incumbent businesses, leading to a diminishment of their market share.<sup>557</sup>

However, it is imperative to acknowledge that while disruptive innovations usher in transformative benefits, they can also constitute a source of perturbation for enterprises tethered to legacy technologies.<sup>558</sup> For instance, with the advent of digital cameras, these innovations presented a markedly more cost-effective and user-friendly alternative to their film-based counterparts.<sup>559</sup> This transition precipitated a contraction in the demand for film cameras, thereby introducing a disruptive dynamic within the film industry.<sup>560</sup> However, business proprietors exhibiting reluctance to integrate novel technologies into their operations, particularly when their enterprises are deeply enmeshed with established technological infrastructures, often harbor apprehensions about the potentially disruptive impact of these emergent technologies.<sup>561</sup> They apprehensively anticipate that adopting these technologies could culminate in migrating their customer base to nascent businesses that pivot around these transformative technologies.<sup>562</sup>

The conceptual framework of disruptive innovation theory holds the potential to explicate and refine the CHIPS Act.<sup>563</sup> Disruptive innovation theory, rooted in business scholarship, delineates how nascent technologies engender fresh markets, concurrently supplanting established ones.<sup>564</sup> Characteristically, disruptive innovations exhibit enhanced cost-effectiveness and user-friendliness

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557. See Clayton M. Christensen et al., *Disruptive Innovation: An Intellectual History and Directions for Future Research*, 55 J. MGMT. STUD. 1, 9 (2018) (“The third source of insight came from Adner and colleagues’ use of mathematical models of asymmetric preferences to show that, as product performance improves, overlap between different market segments increases.”) (Citation omitted).

558. *Id.* at 20 (“Early theoretical formulations were decidedly pessimistic, suggesting that incumbents typically ignore or retreat from disruptive encroachments.”).

559. See Henry C. Lucas Jr. & Jie Mein Goh, *Disruptive Technology: How Kodak Missed the Digital Photography Revolution*, 18 J. STRATEGIC INFO. SYS. 46, 46 (2009) (“The digital camera combined with information and communications technologies (ICT), specifically the capabilities of the computer to store and display photographs, and the Internet to transmit them, transformed the major customer processes associated with photography.”).

560. See *ibid.* (discussing how digital cameras disrupted the film camera industry).

561. See *ibid.* (“Kodak’s middle managers, culture and rigid, bureaucratic structure hindered a fast response to new technology which dramatically changed the process of capturing and sharing images.”).

562. See Christensen et al., *supra* note 557 at 9 (“In other words, because incumbents prioritize their existing customers, they value sustaining innovations over disruptive innovations; they may even ignore nascent disruptive threats that arise within separate resource networks.”).

563. See, e.g., Luc Van den hove, *Why Our Chip Strategy Will Determine Our Future*, IMEC (Oct. 3, 2023), <https://www.imec-int.com/en/articles/why-our-chip-strategy-will-determine-our-future> [perma.cc/JT92-N7GK] (“The challenges are becoming more complex, and so are their respective solutions, as each requires disruptive innovations in chip technology.”); Charles Wessner & Thomas Howell, *Implementing the CHIPS Act: Sematech’s Lessons for the National Semiconductor Technology Center*, CTR. FOR STRATEGIC AND INT’L STUD. (May 19, 2023), <https://www.csis.org/analysis/implementing-chips-act-sematechs-lessons-national-semiconductor-technology-center> [https://perma.cc/NB75-BLFS] (describing strategies for the implementation of the CHIPS and Science Act).

564. See Steven Si & Hui Chen, *A Literature Review of Disruptive Innovation: What It Is, How It Works and Where It Goes*, 56 J. ENG’G & TECH. MGMT. 4, 4 (2020), (“Then, as the attributes of disruptive products or services are gradually improved to a certain extent over time, they would ultimately come to appeal to mainstream customers, and thus would gradually take over the market share of mainstream market from, or even replace the dominant positions of the incumbents.”).

compared to extant technologies, often targeting previously untapped clientele or novel sectors within existing markets.<sup>565</sup>

Leveraging disruptive innovation theory, the CHIPS Act is strategically poised to undergird the evolution of pioneering semiconductor technologies, which bear the potential to engender transformative shifts within extant markets.<sup>566</sup> This is palpable through the Act's provision of funding for research endeavors germane to novel paradigms in chip production, such as 3D chip stacking and chiplet technology.<sup>567</sup> The Act is also calibrated to buttress the domestic production of semiconductor chips.<sup>568</sup> This trajectory could incite the inception of nascent markets for domestically manufactured chips, as exemplified by the burgeoning domain of autonomous vehicular technologies.<sup>569</sup>

Disruptive innovation theory emerges as a potent analytical apparatus for apprehending and navigating the evolving contours of the semiconductor industry. The CHIPS Act signifies a substantial investment in the U.S. semiconductor domain;<sup>570</sup> hence, it is incumbent to ensure that the Act is optimally configured to underwrite the maturation and production of transformative semiconductor technologies. In this vein, several specific instances of how disruptive innovation theory might inform revisions to the CHIPS and Science Act are conceivable.<sup>571</sup> This will be discussed in the recommendation section of this article.

## 2. *Path Dependency Theory*

Another theoretical framework shedding light on the reluctance of businessmen to adopt new technologies is the Path Dependency Theory.<sup>572</sup> This theoretical construct delineates how businesses can become entrenched within a

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565. See generally *id.* (discussing how disruptive innovations that are more cost-effective and user-friendly are established in low-end or untapped markets during the entry phase).

566. See, e.g., Andrew A. King & Baljir Baartartogtokh, *How Useful is the Theory of Disruptive Innovation?*, MIT SLOAN MANAGEMENT REV., at 81 (2015) (“In other cases, our experts doubted that incumbent organizations possessed the capabilities needed to compete with a disruptive entrant.”).

567. See, e.g., Shivakumar et al., *supra* note 28 (“The research center envisioned by DARPA will focus on 3D heterogeneous integrated (3DHI) microsystems, which feature the integration of diverse chip types into a single package for dramatically improved performance.”).

568. See *ibid.* (discussing measures the CHIPS Acts takes to bolster domestic production of semiconductor chips).

569. See, e.g., *Arm Reveals Next-Gen Chip Designs to Accelerate Automated Driving*, TECH MONITOR (Mar. 14, 2024), <https://www.techmonitor.ai/digital-economy/ai-and-automation/arm-reveals-next-gen-chip-designs-to-accelerate-automated-driving?cf-view> [perma.cc/63UT-V7MJ] (“Arm has unveiled new-generation chip designs it believes will turbocharge the development of automated driving.”); *Biden-Harris Administration Announces CHIPS Preliminary Terms with Microchip Technology to Strengthen Supply Chain Resilience for America’s Automotive, Defense, and Aerospace Industries*, U.S. DEPT. COM. (Jan. 4, 2024), <https://www.commerce.gov/news/press-releases/2024/01/biden-harris-administration-announces-chips-preliminary-terms-microchip> [https://perma.cc/3AK7-NPS2].

570. See Shivakumar et al., *supra* note 28 (discussing the investments the CHIPS Act makes for the semiconductor industry).

571. See *infra* Part VI (discussing the impact disruptive innovation theory may have on potential revisions to the CHIPS and Science Act).

572. Kurt Dopfer, *Toward a Theory of Economic Institutions: Synergy and Path Dependency*, 25 J. OF ECON. ISSUES 535, 540 (1991).

particular technological trajectory.<sup>573</sup> This entrenchment may arise from substantial investments in extant technologies or the cultivation of specialized skills and expertise among the workforce tethered to established technologies.<sup>574</sup>

The path dependency theory delineates the manner in which businesses can become ensnared within a specific technological trajectory.<sup>575</sup> This entrenchment may result from substantial investments in established technology or the cultivation of specialized competencies and expertise among the workforce tethered to prevailing technologies.<sup>576</sup> Once an enterprise becomes entrenched within a particular technological trajectory, transitioning to a novel technological paradigm becomes a formidable endeavor, fraught with complexity and cost.<sup>577</sup> This arises from the imperative to overhaul existing equipment and necessitate comprehensive workforce retraining.<sup>578</sup> Consequently, businesses may avoid embracing new technologies, even when the latter proffer substantial advantages.<sup>579</sup>

The Path Dependency Theory elucidates how businesses may become entrenched within a specific technological trajectory, primarily due to substantial investments in extant technology or the cultivation of specialized skills and expertise among the workforce associated with established technologies.<sup>580</sup> Consequently, certain enterprises may resist integrating new

573. See *id.* at 541 (“The initial phase of the process may be defined by a bifurcation regime that shows chaotic features. Already small changes in an actor’s behavior may have large macroscopic consequences for the resulting process.”).

574. See *id.* at 540–41 (“Individual behaviors receive increasingly the status of a norm, that is of an order parameter, that determines individual behaviors. The causation between micro and across is . . . typically circular.”).

575. See Adrian Kay, *A Critique of the Use of Path Dependency in Policy Studies*, 83 PUB. ADMIN. 553, 553 (2005) (“A process is path dependent if initial moves in one direction elicit further moves in that same direction; in other words the order in which things happen affects how they happen; the trajectory of change up to a certain point constrains the trajectory after that point.”).

576. See *id.* at 563 (“As Arrow points out, significant sunk costs and sequencing arguments are sufficient to construct path dependency stories in the economics of technology.”).

577. See, e.g., Robert Cox, *The Path-Dependency of an Idea: Why Scandinavian Welfare States Remain Distinct*, 38 SOC. POL’Y & ADMIN. 204, 208 (2004) (“[P]olicy paradigms have a powerful effect on people’s thoughts and expectations, and [they] are reluctant to alter their paradigmatic views, sometimes even in the face of overwhelming evidence that does not fit the paradigm.”).

578. See Castaldi et al., *supra* note 552 (“The structure and rigidity of organizational memory, as well as the processes of interpretation, information retrieval and action formation of organizations, are fundamental sources of path dependence.”); Pablo Illanes et al., *Retraining and Reskilling Workers In the Age of Automation*, MCKINSEY (Jan. 22, 2018), <https://www.mckinsey.com/featured-insights/future-of-work/retraining-and-reskilling-workers-in-the-age-of-automation> [<https://perma.cc/3XKB-7ZZR>] (“[E]xecutives increasingly see investing in retraining and “upskilling” existing workers as an urgent business priority—and they also believe that this is an issue where corporations, not governments, must take the lead.”).

579. See Stephen Redding, *Path Dependence, Endogenous Innovation, and Growth*, 43 INT’L ECON. REV. 1215, 1215 (2002) (“An extreme example is “technological lock-in,” where agents continue to employ an existing technology even though potentially more productive technologies could be formed.”); *Why Do Large Companies Fail to Adopt New Technologies?*, WARACLE (Aug. 4, 2020), <https://waracle.com/insights/digital-transformation/why-do-large-companies-fail-to-adopt-new-technologies/> [<https://perma.cc/Z35F-7DBY>] (“Established businesses tend to focus on keeping costs down and maintaining existing systems and technologies for as long as possible.”).

580. Dopfer, *supra* note 572.

semiconductor technologies, notwithstanding their potential advantages.<sup>581</sup> This hesitancy arises from the realization that transitioning to new semiconductor technologies necessitates the replacement of existing equipment and retraining personnel.<sup>582</sup>

Once an enterprise becomes locked into a particular technological path, transitioning to a novel technological paradigm becomes a formidable endeavor, fraught with complexity and cost.<sup>583</sup> This arises from the imperative to overhaul existing equipment and necessitate comprehensive workforce retraining.<sup>584</sup> Consequently, businesses may avoid embracing new technologies, even when the latter proffer substantial advantages.<sup>585</sup>

This theoretical construct finds applicability to the CHIPS Act in various respects. Initially, the Act allocates funding for developing and manufacturing novel semiconductor technologies.<sup>586</sup> However, it is imperative to recognize that the semiconductor industry represents a highly mature sector, with numerous businesses investing in extant semiconductor technologies.<sup>587</sup> This explains why some enterprises may be disinclined to adopt new semiconductor technologies, notwithstanding their potentially substantial benefits.<sup>588</sup> This hesitancy arises from the realization that transitioning to new semiconductor technologies necessitates the replacement of existing equipment and retraining personnel.<sup>589</sup>

Additionally, the CHIPS Act allocates funding for workforce development initiatives to equip workers with the requisite skills for success in the semiconductor industry.<sup>590</sup> Nonetheless, it is crucial to acknowledge that a multitude of businesses have already made significant investments in training their employees in prevailing semiconductor technologies.<sup>591</sup> As a result, certain enterprises may resist integrating new semiconductor technologies, necessitating their workforce to acquire novel skill sets.<sup>592</sup> This hesitancy emanates from the obligation to make additional investments in retraining personnel, which may be financially burdensome and time-intensive.<sup>593</sup>

The analytical frameworks of path dependency and disruptive innovation offer instrumental tools for comprehending the challenges and opportunities

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581. *Ibid.*; see Ramiro Palma et al., *How the US Can Strengthen the Global Semiconductor Ecosystem*, BOSTON CONSULTING GROUP, (Dec. 8, 2022) <https://www.bcg.com/publications/2022/how-the-us-can-strengthen-the-global-semiconductor-industry> [<https://perma.cc/N2MN-FZ9S>] (Discussing that many companies face obstacles in incorporating the advancements from semiconductor technologies into their existing ecosystems).

582. Dopfer, *supra* note 572.

583. *Ibid.*

584. *Ibid.*

585. *Ibid.*

586. THE WHITE HOUSE, *supra* note 67.

587. See King & Baartartogtokh, *supra* note 566 (discussing the CHIPS Act's ability to bolster the semiconductor technology space).

588. *Id.*

589. *Id.*

590. THE WHITE HOUSE, *supra* note 67.

591. *Id.*

592. Cox, *supra* note 577.

593. See generally Martin Stack & Myles P. Gartland, *Path Creation, Path Dependency, and Alternative Theories of the Firm*, 37 J. OF ECON. ISSUES 487, 489 (2003) (discussing hesitancy among firms to make financial investments in retraining personnel).

associated with the integration of novel technologies facilitated by the CHIPS Act.<sup>594</sup> This landmark legislation holds the potential for a profound impact on the semiconductor industry.<sup>595</sup> However, it is imperative to recognize that the full extent of its influence may necessitate a period of acclimatization within the industry, particularly for businesses deeply entrenched in established technological paradigms.<sup>596</sup> Collectively, these theoretical constructs provide insights into the phenomenon wherein businessmen exhibit reluctance to adopt novel technologies.<sup>597</sup> Their hesitancy is particularly pronounced when their existing enterprises are intricately interwoven with well-established technological frameworks.<sup>598</sup>

### *B. Impact of New Technologies on Global Semiconductor Supply Chain Dynamics*

While multiple patterning with DUV lithography offers a temporary solution for China's chip manufacturing in the face of limitations on acquiring advanced EUV machines, it presents a limited approach to long-term sustainability.<sup>599</sup> Multiple patterning's dependence on numerous processing steps significantly increases production complexity and cost.<sup>600</sup> Additionally, its scalability for future miniaturization becomes problematic.<sup>601</sup> This is where particle accelerator technology emerges as a potentially game-changing alternative. By utilizing particle accelerators as a novel light source, China could bypass the need for EUV machines.<sup>602</sup> This approach holds promise for achieving long-term sustainability in chip manufacturing.<sup>603</sup> Particle accelerators offer the potential for a more streamlined production process and

594. *See ibid.* (discussing the analytical framework of path dependency); *see also* THE WHITE HOUSE, *supra* note 67 (discussing the enactment of the CHIPS act).

595. THE WHITE HOUSE, *supra* note 67 (discussing the CHIPS act).

596. *See* King & Baatartogtokh, *supra* note 566 (discussing the CHIPS Act's ability to bolster the semiconductor technology space).

597. *See* Rod Coombs & Richard Hull, *Knowledge Management Practices' and Path-Dependency in Innovation*, 27 RSCH. POL'Y 237, 237–39 (1998) (discussing path-dependency and other knowledge management practices).

598. *See* Mina Saghafian et al., *Stagewise Overview of Issues Influencing Organizational Technology Adoption and Use*, 12 FRONT. PSYCHOL., Mar. 16, 2021, at 10 (explaining that hesitancy to adopt disruptive technologies can be due to cultural and structural inertia, as well as asymmetric resource allocation, which can prioritize current, profitable technologies over potentially disruptive innovations).

599. *The Dutch will be cautious about chip export bans*, OXFORD ANALYTICA (2023).

600. *See Applied Materials' Innovative Pattern-Shaping Technology Reduces the Cost, Complexity and Environmental Impact of Advanced Chip Manufacturing*, APPLIED MATERIALS, (Feb. 28, 2023), <https://investors.appliedmaterials.com/news-releases/news-release-details/applied-materials-innovative-pattern-shaping-technology-reduces> [<https://perma.cc/94Z7-7CR5>] (explaining the various steps and costs for film patterning).

601. *Id.*

602. *China May Be Constructing EUV Lithography Machines on a Massive Scale*, THE CHINA ACADEMY, (Sept. 21, 2023), <https://thechinaacademy.org/china-may-be-constructing-euv-lithography-machines-on-a-massive-scale/> [[perma.cc/G5MV-Z9ZN](https://perma.cc/G5MV-Z9ZN)] (explaining that China could construct an "EUV factory" to replace ASML's individual EUV lithography machines).

603. *Id.*

the ability to achieve even smaller transistor sizes, paving the way for future advancements in chip technology.<sup>604</sup>

The integration of particle accelerator technology within the domain of chip manufacturing is poised to engender multifaceted repercussions upon the dynamics of the global semiconductor supply chain.<sup>605</sup> One conceivable ramification is potentially cultivating a more variegated and robust global semiconductor supply chain framework.<sup>606</sup> At present, the locus of the global semiconductor supply chain is markedly concentrated within Asian territories, where enterprises domiciled in Taiwan, South Korea, and China collectively command a substantial portion of worldwide semiconductor production.<sup>607</sup> This prospective development promises to foster diversification within the global semiconductor supply chain, enhancing its capacity to withstand perturbations and disruptions.<sup>608</sup>

Another implication pertains to the emergence of a more fiercely contested global semiconductor market.<sup>609</sup> The infusion of particle accelerator technology could potentially lower the barriers to entry for nascent enterprises seeking ingress into the chip manufacturing sphere.<sup>610</sup> Such an outcome would precipitate an augmented competitive milieu within the global semiconductor market, potentially exerting downward pressure on chip prices and fostering a more dynamic marketplace.<sup>611</sup>

Lastly, employing particle accelerator technology in chip production harbors the potential to catalyze the genesis of novel, cutting-edge semiconductor chips characterized by diminutive form factors and heightened operational performance parameters.<sup>612</sup> The integration of particle accelerator technology could be instrumental in ushering in a new epoch of semiconductor innovation, granting rise to a panoply of unrealized products and services.<sup>613</sup>

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604. Ula Chrobak, *Steering and Accelerating Electrons at the Microchip Scale*, STANFORD REPORT, (Feb. 26, 2024) <https://news.stanford.edu/stories/2024/02/accelerator-chip-advance> [<https://perma.cc/S9AB-33CR>] (“There’s the ability to just completely replace every other particle accelerator with something that’s cheaper and smaller.”).

605. See OXFORD ANALYTICA, *supra* note 599 (discussing particle accelerator technology in chip manufacturing and the Dutch’s caution about it).

606. Saif M. Khan et al., *The Semiconductor Supply Chain: Assessing National Competitiveness*, CTR. FOR SEC. & EMERGING TECH., Jan. 2021, at 3.

607. Joanne Chiao, *China and US Bolster Semiconductor Independence as Taiwan’s Foundry Capacity Share Projected to Decline to 41% by 2027, Says TrendForce*, TRENDFORCE, (Dec. 14, 2023) <https://www.trendforce.com/presscenter/news/20231214-11959.html> [<https://perma.cc/2FD2-6BAN>] (explaining the global semiconductor supply chain is mainly concentrated in Asian territories).

608. Sucharita Gopal, et al., *Semiconductor Supply Chain: A 360-Degree View of Supply Chain Risk and Network Resilience Based on GIS and AI*, in SUPPLY CHAIN RESILIENCE: INSIGHTS FROM THEORY AND PRACTICE. Cham: (Sebastian Kummer et al. eds, 2022).

609. See Khan, *supra* note 606, at 3 (discussing the emergence of different countries in the global semiconductor market).

610. Zhang Tong, *China Plans to Build a Giant Chip Factory Driven by Particle Accelerator*, S. CHINA MORNING POST, (Sept. 25, 2023) <https://www.scmp.com/news/china/science/article/3235419/china-plans-build-giant-chip-factory-driven-particle-accelerator> [[perma.cc/D2BS-FWDV](https://perma.cc/D2BS-FWDV)] (discussing the future of semiconductors and their potential).

611. See Khan, *supra* note 606 (discussing the competitiveness of the semiconductor market).

612. Priyadarshi, *supra* note 376.

613. *Id.*

Incorporating particle accelerator technology into chip manufacturing is poised to exert a profound and far-reaching influence on the intricate fabric of global semiconductor supply chain dynamics.<sup>614</sup> Its advent is anticipated to lead to a more diversified, robust, and competitive global semiconductor market and, in tandem, to usher in a new era of advanced semiconductor chip development.<sup>615</sup>

*C. Reforming the CHIPS Act in the U.S. – A General Perspective*

The question of whether the CHIPS Act needs revision entails a nuanced deliberation devoid of facile solutions. This issue demands an assessment of various factors, including the Act's historical efficacy, the semiconductor industry's evolving exigencies, and the U.S.'s broader economic environment.

Some analysts contend that the CHIPS Act presently functions optimally and, thus, warrants no alteration.<sup>616</sup> This viewpoint posits that any revision may instigate undue disruption and dampen incentives for investment in the domestic semiconductor industry.<sup>617</sup> Additionally, an argument asserts that governmental intervention should refrain from favoring particular entities within the market, advocating for the organic evolution of the semiconductor industry without state interference.<sup>618</sup>

However, advocates for revision posit that augmenting funding for research and development, as well as workforce development, is imperative.<sup>619</sup> Additionally, proponents contend that a revision should be geared towards bolstering the production of sophisticated chips, particularly those integral to artificial intelligence and machine learning applications.<sup>620</sup> A further perspective asserts that a revision should encompass measures addressing apprehensions regarding national security, potentially entailing an augmented domestic production of chips.<sup>621</sup>

Should a revision of the CHIPS Act be deemed necessary, several avenues for reform emerge. These include augmenting funding allocations for research and development alongside workforce development initiatives.<sup>622</sup> Alternatively,

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614. *Id.*

615. *Id.*

616. See James Pethokoukis, *Is the CHIPS Act Really Working?*, FASTER PLEASE, (May 10, 2024), <https://fasterplease.substack.com/p/is-the-chips-act-really-working> [<https://perma.cc/JM2V-2EL7>] (discussing the author's opinion that the CHIPS Act has been successful in its implementation).

617. *Id.*

618. See SUTTER ET AL., *supra* note 72, at 1–3 (discussing the government's involvement in the semiconductor industry).

619. See DARMODY, *supra* note 88, at 3 (discussing the importance of funding under the CHIPS act).

620. *Ibid.*; Sebastian Göke et al., *Scaling AI in the Sector That Enables It: Lessons for Semiconductor-Device Makers*, MCKINSEY & COMPANY (Apr. 2, 2021), <https://www.mckinsey.com/industries/semiconductors/our-insights/scaling-ai-in-the-sector-that-enables-it-lessons-for-semiconductor-device-makers> [<https://perma.cc/FZ8V-D2GL>].

621. Göke, *supra* note 620.

622. See generally Vishnu Kannan and Jacob Feldgoise, *After the CHIPS Act: The Limits of Reshoring and Next Steps for U.S. Semiconductor Policy*, CARNEGIE (Nov. 22, 2022), <https://carnegieendowment.org/research/2022/11/after-the-chips-act-the-limits-of-reshoring-and-next-steps-for-us-semiconductor-policy?lang=en> [[perma.cc/T59W-NV9Y](https://perma.cc/T59W-NV9Y)] (“To begin addressing this issue, the White House and Commerce

a focus on bolstering the production of advanced chips, particularly those germane to artificial intelligence and machine learning, is posited.<sup>623</sup> Addressing national security concerns by mandating an increased proportion of domestically produced chips is a further potential avenue for reform.<sup>624</sup> Moreover, incentivizing domestic investment in new chip manufacturing facilities through tax breaks or analogous mechanisms is another conceivable strategy.<sup>625</sup> Establishing a government-endorsed consortium for advancing novel chip technologies is yet another prospective reform avenue.<sup>626</sup>

The current state of the U.S. semiconductor industry necessitates comprehensive legislative revisions to bolster domestic production, technological advancement, and national security. One potential avenue for improvement lies in increasing research funding for transformative semiconductor technologies.<sup>627</sup> This would accelerate innovation and ensure American leadership in crucial chip development.<sup>628</sup> Additionally, the legislation could be recalibrated to prioritize the manufacturing of cutting-edge chips within the U.S., potentially through targeted incentives or direct government investment.<sup>629</sup>

Furthermore, strengthening national security through domestic chip production should be a central tenet of the revised legislation. This could involve mandating a minimum percentage of domestically produced chips for government agencies or implementing policies that incentivize private companies to onshore their manufacturing operations. However, it is crucial to maintain a high degree of flexibility for chip suppliers to navigate complex geopolitical realities.<sup>630</sup> Recent actions, such as the U.S. Department of Commerce granting exemptions to major chipmakers supplying China, demonstrate the need for a nuanced approach that balances national security concerns with economic realities.<sup>631</sup>

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Department should convene leading scholars to explore how complementary economic policies and initiatives can create opportunity for the parts of the domestic labor force that are struggling.”)

623. See generally BLEVINS ET AL., *supra* note 38, at 1–4 (discussing the enhancements in the production of advanced chips for AI and machine learning by highlighting initiatives like the NSTC, strategic export controls, and concerns over U.S. competitive disadvantages in the semiconductor industry.).

624. See Kannan and Feldgoise, *supra* note 622 (discussing a hypothetical if China were to invade Taiwan).

625. See *id.* (“Government subsidies, loan guarantees, and tax credits are behind much of this rearrangement, and the chipmakers themselves have said that subsidies are the single most important factor in deciding where they will stand up new fabrication capacity.”).

626. See *id.* (stating that a government consortium could be a viable supplement to domestic chip production).

627. See Blevins et al., *supra* note 38, at 1–4 (discussing the CHIPS Act’s provisions aimed at ensuring U.S. leadership in semiconductor technology through various R&D initiatives, which collectively received significant funding).

628. See *Semiconductors*, NIST, <https://www.nist.gov/semiconductors> [perma.cc/J7UX-BK89] (last visited Sept. 24, 2024) (“Moves are afoot to boost U.S. semiconductor manufacturing, research innovation and supply chain security.”).

629. See Kannan and Feldgoise, *supra* note 622 (discussing potential need to appropriate funds toward chip production).

630. See *id.* (discussing international effects of U.S. chip production).

631. Joyce Lee, *South Korean Firms Get Indefinite Waiver on US Chip Gear Supplies to China*, REUTERS (Oct. 10, 2023 12:19 PM), <https://www.reuters.com/technology/samsung-sk-hynix-wont-need-approvals-supply-us-chip-gear-china-yonhap-2023-10-09/> [https://perma.cc/P4D8-ZQNS].

In conclusion, a multifaceted approach encompassing increased research funding, targeted manufacturing incentives, and a strategic balance between domestic production and global engagement is necessary to revitalize the U.S. semiconductor industry and ensure its long-term competitiveness and security.

*D. Reforming the CHIPS Act in the U.S. – A Focus on Particle Accelerator Technology*

The competitiveness and national security of the U.S. semiconductor industry hinges on fostering innovative technologies like particle accelerators in chip manufacturing.<sup>632</sup> While the existing CHIP Act offers support,<sup>633</sup> several strategic revisions can significantly enhance its efficacy in this domain.

Firstly, dedicated funding allocation is crucial to the development of specialized equipment and tools tailored to the unique challenges of integrating particle accelerators into chip fabrication processes.<sup>634</sup> This targeted investment will provide the necessary infrastructure to overcome these technical hurdles and pave the way for wider adoption.<sup>635</sup>

Secondly, substantial support for research and development initiatives is essential. Encouraging collaborative partnerships between government, industry, and academia can significantly accelerate progress.<sup>636</sup> Such collaborations combine diverse expertise and resources, expediting particle accelerator chips' technological maturation and commercialization.<sup>637</sup> Augmenting overall funding for domestic semiconductor manufacturing and research is crucial. However, prioritization is key, with resources directed towards establishing new fabrication facilities and incubating cutting-edge technologies like particle accelerators.<sup>638</sup> This strategic allocation ensures efficient utilization of funds to address critical challenges and opportunities.<sup>639</sup>

Additionally, reconsidering funding restrictions based solely on geographical location could be beneficial. While national security concerns are

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632. See Kannan and Feldgoise, *supra* note 622 (discussing national security implications); Kutsaev, *infra* note 634 at 161 (discussing the growth of particle accelerator technology and its effects on the industry).

633. See DARMODY, *supra* note 88, at 14, 16 (2023) (discussing the CHIPS Act funding for Department of Energy technology hubs to further innovation in the energy sector).

634. See S. V. Kutsaev, *Advanced Technologies for Applied Particle Accelerators and Examples of their Use*, 66 *TECH. PHYSICS* 161, 172 (2021) (“[T]he price factor plays an important role in this case.”).

635. See Blevins et al., *supra* note 38, at 1–4 (discussing how investments in manufacturing capacity and technology upgrades are essential to overcoming current challenges and promoting wider adoption of advanced chip technologies).

636. See *ibid.* (discussing a \$52.7 billion semiconductor initiative that emphasize collaboration in research, workforce development, and international partnerships to enhance supply chain resilience and technological advancement).

637. *Stronger Together: Investing in Collaboration Amid the Resurgence of the U.S. Semiconductor Industry*, MERCK KGAA (Aug. 6, 2024) <https://www.emdgroup.com/en/the-future-transformation/stronger-together-investing-in-collaboration-amid-the-resurgence-of-the-us-semiconductor-industry.html> [<https://perma.cc/WSH7-XPPY>].

638. See, e.g., James Leggate, *Feds Offer Texas Instruments \$1.6B to Support Construction of Three Fabs*, ENR (Aug. 19, 2024), <https://www.enr.com/articles/59148-feds-offer-texas-instruments-16b-to-support-construction-of-three-fab-plants> [<https://perma.cc/LPW4-7ZS>] (providing an example of investment in new fabrication facilities).

639. See *id.* (addressing how investment benefits production and creates jobs in the industry).

valid, a more nuanced approach fostering international collaboration and knowledge exchange within responsible frameworks could accelerate overall technological progress.<sup>640</sup> Finally, workforce development is crucial alongside technological advancements. Investing in training programs will equip the workforce with the necessary skills and expertise to operate and maintain this complex technology, ensuring a skilled talent pool for the future.<sup>641</sup>

These measures can significantly advance the government's role in preserving U.S. leadership in particle accelerator chip manufacturing. The CHIPS Act requires revisions to earmark funds specifically for research and development in this area.<sup>642</sup> The Act needs to be reset to bolster domestic semiconductor manufacturing and research, emphasizing advancements in novel technologies like particle accelerators. This necessitates revisions that profoundly influence research and development in this domain through various channels.<sup>643</sup> A portion of the allocated funding should be directed toward particle accelerator research, empowering researchers to innovate and develop novel applications in chip manufacturing.<sup>644</sup>

Furthermore, the Act needs revisions to forge new alliances between government, industry, and academia. The revised Act can unite diverse experts for collaborative research and development efforts by establishing funding provisions for research centers and consortiums.<sup>645</sup> These synergistic partnerships will expedite the development of cutting-edge particle accelerator technology for chip production.<sup>646</sup> Additionally, the Act needs to stimulate research by catalyzing an increased demand for skilled professionals in this field. As the industry embraces particle accelerator technology, a surge in demand for engineers, scientists, and technicians is anticipated.<sup>647</sup> The CHIPS Act should

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640. See Fuller, *supra* note 1 (describing the chip war, and the United States collaboration with other countries to advance chip technology).

641. See, e.g., *Brown Announces New Investment in Semiconductor Innovation and Job Training at Central State University*, SHERROD BROWN U.S. SENATOR FOR OHIO (Sept. 20, 2024), <https://www.brown.senate.gov/newsroom/press/release/sherrod-new-investment-semiconductor-innovation-job-training-central-state-university> [<https://perma.cc/H2GC-2MLB>] (providing an example of government investment in training programs); Blevins et al., *supra* note 38, at 1–4 (discussing the requirement for applicants to establish partnerships with educational institutions for workforce training directly aims to develop a skilled talent pool capable of operating and maintaining advanced semiconductor technologies).

642. See generally CHIPS and Science Act of 2022, 42 U.S.C.A. § 18643 (2022) (making no mention particle accelerators).

643. See generally Kannan and Feldgoise, *supra* note 622 (discussing goals for revisions).

644. See generally CHIPS and Science Act of 2022 § 18643(b) (providing the basis for which the proposed revision would focus on).

645. See generally Kannan and Feldgoise, *supra* note 622 (discussing the benefits of consortiums).

646. See Kutsaev, *supra* note 634 (discussing the benefits of particle accelerator technology in chip manufacturing).

647. See *Workforce Development*, NIST (Sept. 17, 2024) <https://www.nist.gov/chips/workforce-development> [<https://perma.cc/5F72-TQS7>] (“The success of CHIPS for America will require collaboration between businesses, governments, education and training providers, economic and workforce development organizations, unions, community-based organizations, and other supporting organizations to help recruit, train, hire, and retain a highly-skilled semiconductor and construction workforce.”).

allocate funding for workforce development programs to equip individuals with the requisite skills for thriving in the semiconductor industry.<sup>648</sup>

Ultimately, the success of revising the CHIPS and Science Act rests upon political deliberation. The Biden administration and Congress must carefully evaluate the arguments for and against revision, considering both economic prosperity and national security.<sup>649</sup> By enacting these strategic revisions, the CHIPS Act can be effectively leveraged to propel the development and adoption of particle accelerator technology, ultimately strengthening the U.S. semiconductor industry and fostering global technological leadership.<sup>650</sup>

## VII. CONCLUDING REMARKS

China's prevailing initiative is to establish an effective way to use lithographs based on multiple patterning skills.<sup>651</sup> At the same time, China is actively exploring a novel light source for lithography machines, integrating particle accelerators and SSMB technologies.<sup>652</sup> This adoption of technologies, of multiple patterning and particle accelerators, has the potential to reconfigure the competition in the global semiconductor industry substantively.<sup>653</sup> China's strategic objective is to domesticate the manufacturing of chips, thereby mitigating dependencies on foreign technological entities.<sup>654</sup> Central to this pursuit is the aspiration to assume a preeminent position in the semiconductor fabrication process, particularly in cutting-edge technologies such as 2nm chip manufacturing.<sup>655</sup>

Both the CHIPS Act and the EU Chips Act are important pieces of legislation that aim to strengthen the semiconductor industries of the U.S. and the EU.<sup>656</sup> On a comparative basis, the CHIPS Act in the U.S. provides more funding than the European Chips Act and has a stronger focus on manufacturing.<sup>657</sup> The EU Chips Act, on the other hand, has a stronger focus on research and development, emphasizing collaborative international efforts and innovative technologies.<sup>658</sup> Both acts also differ in their approach to particle accelerator technology.<sup>659</sup> The CHIPS Act does not mention particle accelerator technology but provides semiconductor research and development funding.<sup>660</sup>

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648. *See id.* ("Increased funding for semiconductor R&D will lead to the discovery and development of new products and technologies. This will help to create more job opportunities and help to attract more workers to the field.")

649. THE WHITE HOUSE, *supra* note 15.

650. *Id.*

651. Shilov, *supra* note 248.

652. Priyadarshi, *supra* note 375.

653. Shilov, *supra* note 248; Priyadarshi, *supra* note 375.

654. Chad P. Bown, *How the United States Marched The Semiconductor Industry into Its Trade War With China*, 24 EAST ASIAN ECON. REV. 4, 367 (Dec. 2020).

655. Priyadarshi, *supra* note 375.

656. Sujai Shivakumar et al., *supra* note 28.

657. *Supra* text accompanying notes 16, 154–156.

658. Wills, *supra* note 217, at 27–28; Shivakumar et al., *supra* note 28.

659. CHIPS and Science Act, Pub. L. No. 117-167, § 10109, 136 Stat. 1366; Kannan and Feldgoise, *supra* note 622.

660. Wang et al., *supra* note 2.

The EU Chips Act, on the other hand, specifically mentions particle accelerator technology and its potential to revolutionize chip manufacturing.<sup>661</sup>

To support the development of new semiconductor technologies and to invest in research and development to improve the efficiency and sustainability of the global semiconductor supply chain, the U.S. and the EU should work together to develop and implement global semiconductor supply chain security standards. This would help to protect the global semiconductor supply chain from cyberattacks and other threats.<sup>662</sup>

By incorporating the recommendations as stipulated in this article, the U.S. and the EU can strengthen their semiconductor industries and reduce their reliance on foreign suppliers to some extent. This will help to ensure that they remain at the forefront of semiconductor technology and that they can develop and deploy the products and services of the future.<sup>663</sup>

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661. CHIPS and Science Act, Pub. L. No. 117-167, § 10109, 136 Stat. 1366.

662. See Kannan and Feldgoise, *supra* note 622 (detailing expert opinion on how chip manufacturing should aim to withstand cyberattacks).

663. See generally Verheyden et al., *supra* note 157; THE WHITE HOUSE, *supra* note 15 (describing the goal for the United States to be leaders in the industry).